ISBN: 978-3-95450-208-0 doi:10.18429/JACoW-IPAC2019-THPTS060

SIRIUS DIGITAL LLRF

A. Salom, F. Perez, CELLS – ALBA, Cerdanyola del Vallès, Spain
R. H. A. Farias, F. K. G. Hoshino, A. P. B. Lima, Brazilian Synchrotron Laboratoy (LNLS), Campinas, Brazil

Abstract

Sirius is a Synchrotron Light Source Facility based on a 4th generation low emittance storage ring. The facility is presently under construction in Campinas, Brazil, and comprises a 3 GeV electron storage ring (SR), a full energy booster synchrotron and a 150 MeV Linac. The Booster RF system is based on a single 5-cell cavity driven by a 45 kW amplifier at 500MHz and is designed to operate at 2 Hz rate. The storage ring RF system will start with 1 normal conducting 7-cell cavity. In the final configuration, the system will comprise 2 superconducting cavities, each one driven by a 240 kW RF amplifier. A digital LLRF system based on the ALBA LLRF has been designed and commissioned to control 3 different types of cavities: 2 normal conducting single cell cavities, one multi-cell cavity driven by 2 amplifiers and one superconducting cavity driven by 4 amplifiers. The first LLRF System will be installed and commissioned in the Sirius Booster in 2019. The performance of the control loops in the high power RF lab, together with other utilities of the system like automatic start-up, conditioning, fast interlocks and post-mortem analysis will be presented in this paper, as well as possible upgrades for the future.

INTRODUCTION

The Sirius Light Source Facility is under construction at LNLS, in Campinas, Brazil. It is based on 5BA Lattice capable to achieve ultralow emittance values (0.28mm.rad). The Sirius injector consists of a 150 MeV linear accelerator and a full energy synchrotron Booster installed in the same tunnel and concentric with the storage ring. The installation and commissioning of Linac was finished in 2018 and this year, the Booster and SR will be commissioned [1].

The final RF System of the SR will be composed of two superconducting cavities powered by two 240 kW Solid State Power Amplifiers (SSPA) and working at 500MHz, but for the commissioning and initial operation a 7-cell PETRA cavity will be used. On the other hand, the Booster RF system will have a 5-cell PETRA Cavity powered by a SSPA.

A Digital Low Level RF (DLLRF) capable to control these three types of cavities has been designed and fabricated based on the ALBA System.

The ALBA DLLRF is based on commercial FPGAs. In the first adaptations of this system for Max-IV and Diamond [2, 3], a uTCA board from Nutaq (Perseus 601X) with Virtex-6 FPGA motherboard with ADCs and DACs FMC boards were used [3]. uTCA is an open standard modular hardware complementary to AdvancedTCA, targeted for low start-up cost. However, for the Sirius LLRF a stand-alone board was employed, the Picodigitizer from Nutaq. This new board has the same processing capabilities than the Perseus, but lacks the uTCA backplane that allows fast communication between boards connected to the same chassis, that so far, had not been used in previous ALBA LLRF versions. With this new stand-alone system, there is no need for AMC chassis nor host PC, reducing the HW cost of the system by 50% while maintaining the same functionalities and processing capabilities. The communications with the FPGA motherboard are done via Giga-Ethernet and accessing an embedded Linux processor of the FPGA.

SIRIUS DLLRF HARDWARE

The main HW components of Sirius DLLRF are:

- Picodigitizer: FPGA mother board + FMC boards for ADCs and DACs + mezzanine Mestor with digital GPIO bus.
- Front Ends for RF Drives up and down conversion.
- Local Timing for LO generation and FPGA clock synchronization with MO reference.
- Patch Panels: connector and levels adapters between DLLRF and RF plants sub-systems.

Figure 1 shows the main hardware components of DLLRF and the interaction between the different RF and digital signals of the sub-systems: Front Ends, Digital Patch Panel and Picodigitizer.

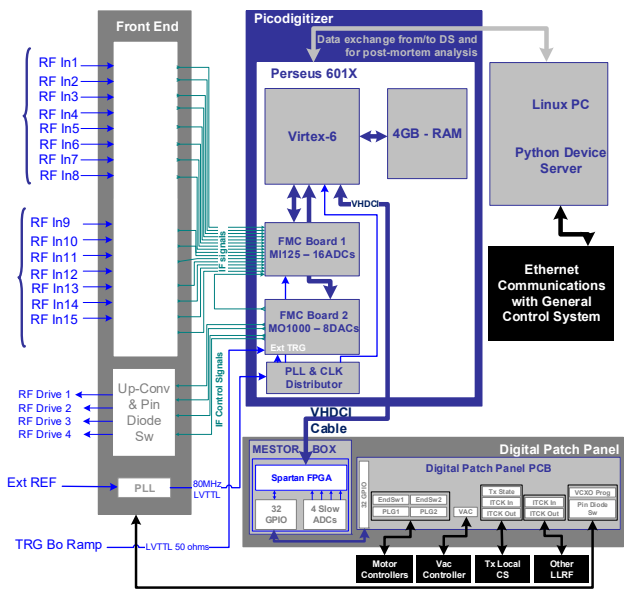

Figure 1: Main hardware components of Sirius DLLRF.

Figure 2 and Fig. 3 show pictures of the main HW components of the Sirius DLLRF prototype used in the High

ISBN: 978-3-95450-208-0 doi:10.18429/JACoW-IPAC2019-THPTS060

Power RF lab of Sirius for conditioning the Booster 5-cells PETRA Cavity.

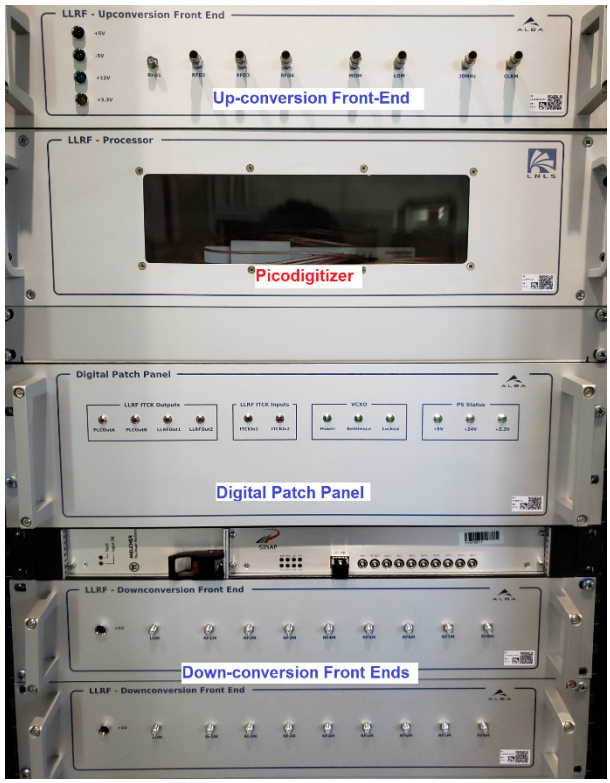

Figure 2: Front Panel of DLLRF Setup of High Power RF lab of Sirius.

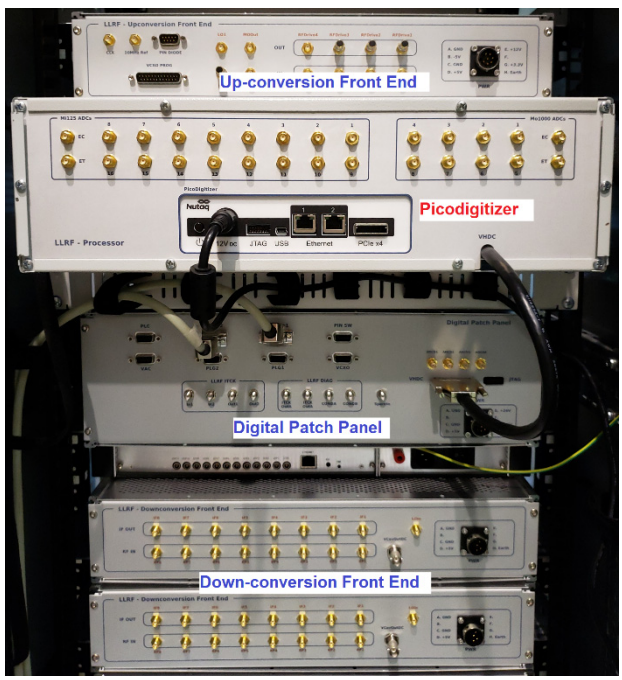

Figure 3: Rear Panel of DLLRF Setup of High Power RF lab of Sirius.

Digital FPGA Motherboard: Picodigitizer

The Picodigitizer board has a Virtex-6 SX315T FPGA and two FMC boards, one with 16 ADC channels of 14 bits capable to operate up to 125MHz and another FMC board with 8 DACS of 16bits 250MSPS. The resolution of the ADCs are better than 0.06% rms in amplitude and 0.04º rms in phase and the signal to noise ratio is better than 70dB [3].

The Picodigitizer also includes a mezzanine board, the Mestor expansion board, with a 32 bits GPIO bus that is used for digital interfaces with other sub-systems of the RF plants like motor controller, vacuum controllers, timing and control system. The Digital Patch Panel adapts the level of the GPIO bus signals (LVTTL), to whatever digital level required by the other subsystems: dry contact, open collector, TTL, 24, etc.

Front Ends and Timing System

The down-conversion front ends transform the 500MHz signals of the RF plant into 20.81 MHz signals (Intermediate Frequency – IF), while the up-conversion Front End transforms the 20.81 MHz control signals provided by the DACs of the digital platform into 500MHz RF signals.

The IF signals of the Front Ends are sampled by the Picodigitizer at 4 times the IF frequency, condition required to perform an IQ-demodulation.

The 20.81 MHz IF required to generate the Local Oscillator of 479.18MHz (MO – IF) is provided by a Frequency Divider (Valon Frequency Divider 3010 [4]). The input of this device is the MO and it provides up to 3 outputs whose frequency is equal to the input frequency divided by integers between 1 and 32. The previous ALBA LLRF Timing system used a programmable PLL with a narrow VCXO clock. The main advantage of this new frequency divider is that no programming of PLL is needed (rebooting the system or shutdowns have no effect) and there is no limitation by the bandwidth of the VCXO that may result in unlocked PLL status when changing the MO frequency for orbit adjustment requirements. The Valon Frequency Divider also provides the clock for FPGA and ADCs/DACs whose frequency is equal to the MO divided by 6.

The Front End supplies SMA test points as shown in Fig. 2 for testing purposes. They are connected through bidirectional couplers to the main RF signals of the DLLRF.

SIRIUS DLLRF FIRMWARE

Cavities Configuration

Sirius DLLRF can be configured to operate with different types of cavities. The standard operation will provide 4 RF Drives for the 4 transmitters powering one Super Conducting Cavity. It will also generate the control output for the plunger responsible of the resonance frequency adjustment of the cavity.

For the Booster Operation, the LLRF will provide one RF Drive and two control outputs to control the two plungers of the multi-cell cavity.

A third configuration is available to control two cavities independently by one LLRF. In this case, the LLRF can provide two RF Drives for each cavity and two independent output controls for the plungers of each cavity.

ISBN: 978-3-95450-208-0 doi:10.18429/JACoW-IPAC2019-THPTS060

IQ Digital Demodulation

All IF signals are sampled by the ADCs of the Picodigitizer boards at 83.275MHz. The sampled signals are demultiplexed and signed inverted when required to perform an IQ Digital Demodulation. These outputs are also sent to a multiplexer so the user can select which RF signals will be controlled. In normal operation, the selected signal will be the cavity voltage, although in some cases like during the conditioning of the cavity, other signals like the Forward Power of the Cavity or the Output of the Amplifier may be more convenient to control.

PI Loops for Voltage Control: IQ vs Polar

Taking advantage of the large processing resources of the Virtex-6 FPGA families, two loop strategies were implemented: Polar loops (amplitude and phase) and Rectangular or IQ loops.

The main advantages of IQ Loops compared to Polar loops are smaller group delay and the possibility of using the same PI Loop for both IQ components. The main advantage of the Polar Loops compared to the rectangular loops is that amplitude and phase loops can be enabled/ adjusted independently, establishing different loop bandwidths for the phase loop and for the amplitude loop if needed [5].

The long term stability of the loops have been tested connecting the DLLRF system to the SSPA of the Booster and load. During the second half of 2019 the system will be tested with the 5-cells Booster Cavity and with Beam.Phase Shifters

The demodulated IQ signals are sent to phase shifters to avoid a positive feedback instabilities. Also, for the super conducting cavity configuration, where 4 RF Drives are generated for up to four independent transmitters, a digital phase shifter and gain multiplier is added to the signals prior being sent to the DACs. In this way, any phase delay or cable attenuation can be compensated and maximize the combination of the transmitter outputs.

Booster Ramping

In the Booster Configuration, the RF Drive is ramped at 2Hz rate. The DLLRF allows the definition of a linear ramp with the following parameters: Initial and final voltage amplitude and phase, and ramping times.

The tuning and field flatness loop are only enabled at the top of the ramp and the dynamic range of this ramp can be set up to 30dB.

Tuning Loop and Field Flatness

To keep the resonance frequency of the cavity, a tuning loop compares the phase of the Forward Power of the cavity and the Cavity Voltage. In case the phase difference is outside a certain margin defined by the user (tuning deadband), a plunger is moved inside/outside the cavity body.

In the case of multi-cells cavities, the voltage of two cells are measured and compared. In case there is a difference greater than a certain value (user's defined dead-band) the field-flatness loop will move the two tuners independently in order to flatten the voltage.

For stability reasons, the main tuning loop always takes prevalence with respect the field flatness one.

Automatic Start-up

In order to make easier and faster the recovery of a RF plant, an automatic start-up process was implemented in the DLLRF. In standby state, the LLRF sets the RF Drive to a minimum value defined by the user and it disables all loops until RF power is detected. Once the Tx is ready and delivering power, the LLRF tunes automatically the cavity and after that, the Amplitude and Phase loops are enabled. In the last stage of the automatic start-up the LLRF increases smoothly the RF Drive from low to nominal power. When this is achieved, the LLRF informs the operator the system is ready to start operation with beam.

Automatic Conditioning

To speed up the conditioning process of the cavities, an automatic conditioning utility was implemented: For doing this, a digital output of a Vacuum Gage Controller (VGC) was connected to the GPIO bus of the LLRF. This output is a dry contact that get opened when the vacuum pressure of the cavity is above certain limit and gets closed when the vacuum level is recovered. Depending on the state of this signal, the LLRF automatically increases the Cavity Voltage set point or it remains at the same power level.

Besides this, if required, the RF Drive can also be square modulated at 10Hz. The user can adjust the duty cycle of the modulation and the amplitude at the top and bottom of the square pulse.

Fast Interlocks and Fast Data Logger

The main RF Interlocks of the DLLRF are the reverse power at the different points of the RF plant (cavity, circulator input and output and amplifiers outputs). The main digital interlocks of the DLLRF are Machine Protection System, Vacuum interlocks, End Switches of motor plungers and Transmitter interlocks.

Whenever one of these interlocks is detected, the DLLRF will open the pin diode switches connected to the RF Drives. Besides, it will set the system in standby state (loops disable and DACs input set to minimum values) and it will inform the transmitter and the main machine protection systems.

In addition, the Fast Data Logger (FDL) will also be triggered. This utility consists of a 4GB RAM continuously acquiring data in a circular buffer. When a trigger is raised either on demand or due to an interlock, the acquisition is stopped and the RAM data is sent the host PC for post-mortem analysis

CONCLUSIONS

The DLLRF of Sirius based on commercial FPGA boards was assembled in 2017 and is being commissioned in 2019. The flexibility and modularity of the system has allowed adding extra features to the LLRF that have made easier the operation of the RF systems.

ISBN: 978-3-95450-208-0 doi:10.18429/JACoW-IPAC2019-THPTS060

REFERENCES

[1] A. R. D. Rodrigues *et al.* "Sirius Light Source Status Report" in *Proc. 9th Int. Particle Accelerator Conf. (IPAC'18)*, Vancouver, BC, Canada, Apr.-May 2018, doi:10.18429/JACoW-IPAC2018-THXGBD4

[2] A. Salom, F. Perez, R. Lindvall, L. Malmgren, A. M. Milan, and A. M. Mitrovic, "Digital LLRF for MAX IV", in *Proc. 8th Int. Particle Accelerator Conf. (IPAC'17)*, Copenhagen, Denmark, May 2017, pp. 4037-4039. doi:10.18429/JACoW-IPAC2017-THPAB135

[3] P. Gu *et al.*, "Digital Low Level RF Systems for Diamond Light Source", in *Proc. 8th Int. Particle Accelerator Conf. (IPAC'17)*, Copenhagen, Denmark, May 2017, pp. 4089-4091. doi:10.18429/JACoW-IPAC2017-THPAB152

[4] https://www.valonrf.com/frequency-divider-2ghz.html

[5] A. Salom, E. Morales, and F. Perez, "Development of a DLLRF Using Commercial uTCA Platform", in *Proc. 8th Int. Particle Accelerator Conf. (IPAC'17)*, Copenhagen, Denmark, May 2017, pp. 3631-3634. doi:10.18429/JACoW-IPAC2017-THOAA1