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DESIGN OF ANALOG TO DIGITAL CONVERTER SCHEME FOR HIGH - PRECISION ELECTROMAGNET POWER SUPPLY

Min-Jae Kim†, Jang Hui Han, Seong-Hun Jeong, Young-Gyu Jung, Dong Eon Kim, Hong-Gi Lee, Sangbong Lee, Sojeong Lee, bong-Gi Oh, Hyung Suck Suh, Heung-Sik Kang, Ki-Hyeon Park, PAL, POSTECH, Pohang, Korea
Yoon-Geol Choi, Department of Electrical Engineering, POSTECH, Pohang, Korea
Minsung Kim, Department of Electrical Engineering, Dongguk University, Seoul, Korea

Abstract

This paper deals with the design of an analogue-to-digital converter (ADC) scheme for a highly precise magnet current supply (MPS). The MPSs are requires with stable and precise current specification in range of the ppm. To meet the requirements, the AD circuit is composed of parallel ADCs of low-medium resolution. Digitally, the oversampling and averaging are performed to increase both the effective resolution and the signal to noise ratio (SNR). The implemented AD circuit was improved about 18 dB (32 times oversampling). The MPS applied by the proposed ADC scheme provides more precise control and the stable current within 10 ppm at 200 A. The experiment used a dipole magnet of the PAL-XFEL and its results proved feasibility through precisely measurable DVM3458A (Keysight Co.).

INTRODUCTION

The PAL-XFEL requires high stability of beam energy (< 0.01%), and measurement and steering of beam trajectory to < 2 μm [1]. To meet these requirements, the accelerator facility needs a highly-stable magnet current supply (MPS) with high precision of a few parts per million (ppm). The particle accelerator gallery is afflicted by many sources of noise, so current control within a few ppm is a difficult task. Because of this high noise level, the precision feedback signals cannot be sampled. Among the MPS parts, the resolution of the analog-to-digital (AD) circuit has the greatest effect on the control precision. Therefore, the AD board was designed with parallel analog-to-digital converter (ADC) chips, and its signal grounds are separated to decrease the noise between analogue and digital circuits. In software, oversampling is performed using a DSP that converts the analogue signal into digital with a higher sampling rate than the required period. Then a large amount of sampling data is averaged for each control period. This method increases the signal-to-noise ratio (SNR) in a noisy environment such as the PAL-XFEL gallery.

When the developed ADC scheme is applied to the MPS, it has current stability within 5 ppm and the control precision is confirmed to be in 10 ppm steps. The load of MPS was applied to a dipole magnet of 200A class on the PAL-XFEL. The proposed ADC scheme facilitates precise and stable current control within a few ppm.

DESIGN OF CONTROL SYSTEM FOR NOISE REDUCTION

Configuration of the Control System

The control system (Fig. 1) is divided into a gate driver, ADC & DSP, an interlock, and a power board.

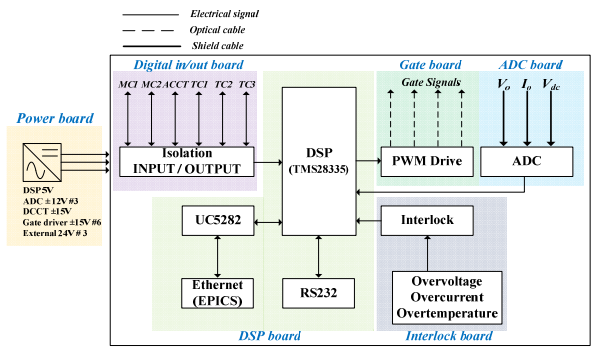

Figure 1: Configuration of the control system.

The control system is modularized (Fig. 2) to simplify maintenance. The DSP board performs main tasks such as current control, PWM generation, communication with other equipment, initial charge, and monitoring.

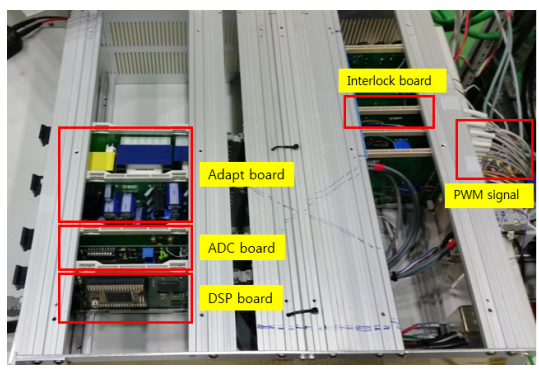

Figure 2: Control board diagram of the MPS.

The PWM signals are conducted to the power stack through optic cables. The interlock circuit has a function of detecting the MPS fault signal and shutting off the PWM output. The power board supplies the control system. The ADC board is the most important part for highly-precise control. For this reason, we provide the cleanest possible

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power supply, and use shielded cables to reduce the effects of noise.

Design of AD Circuits

According to oversampling theorem, it improves resolution of sampling and reduces noise in the noisy environment. To get the accurate signal, high amount of samples are averaged for every specific period.

An oversampling scheme (Fig. 3) is applied to the MPS. During oversampling, the ADC converts an analog to digital at a higher sampling rate than the bandwidth of interest. Combined with suitable digital signal processing like summing and decimation, this method can increase the effective bit resolution of ADC, and improve the signal-to-noise ratio (SNR) [2]. Thus, hardware are designed specifically, and suitable signal processing was adopted.

The current stability was < 10 ppm peak-to-peak for 200-A rated MPS; this limit means that the resolution of ADC for feedback control must be > 17 bit. An AD 977 analog-to-digital converter (Analog Devices Co.) is used, for which the specifications are 16-bit resolution, 200-kHz throughput, and internal reference. The sampled data are averaged in a DSP (TMS320F28335 TI Co) [3]. Whenever the DSP requests the conversion data, the ADC chips send the ADC data through the SPI communication. The data are calculated just before the process in every control period.

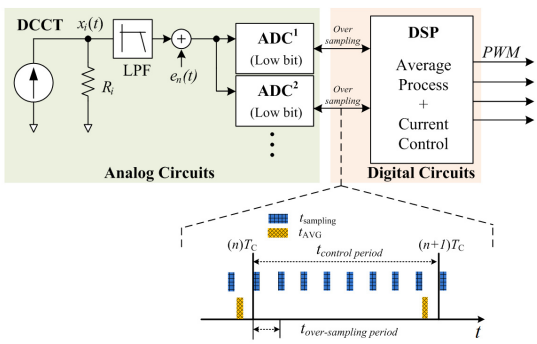

Figure 3: Proposed ADC Scheme and oversampling timing diagram.

A DSP TMS320F28335 (TI Co.) was used to control the duty of the pulse-width-modulation (PWM) and to interface surrounding peripherals. It has six enhanced PWM modules with 150-ps micro-edge-positioning (MEP) technology. Thus, effective PWM resolutions can be increased up to ~ 18 bit. Without MEP, the normal PWM resolution is about 12 bit, which is insufficient resolution of output current to achieve high stability.

EXPERIMENT USING THE DIPOLE MAGNET IN T

Hardware Configurations of the MPS

The MPS is divided into hardware and controller. The hardware is modularized in units of 100 A to in-crease current capacity. The controller is designed to be easy to maintain.

The input (Fig. 4) of the MPS consists of initial charging circuits, a three-phase delta-wye transformer, rectifiers, and an input filter.

The delta-wye transformer of low frequency is applied to make lower DC-link voltage ripple than using only one either a delta transformer or a wye trans-former. The LC filter (Inductance L = 1 mH, Capacitance C = 10 mF) at the input stage is essential to reduce ripple components of line frequency. The DC voltage ripple rectified by the delta-wye transformer is 720 Hz, i.e., twice the input frequency of 360 Hz. The rectifier diodes are constructed in series to eliminate the circulating current caused by the output voltage difference of the delta or the wye transformer.

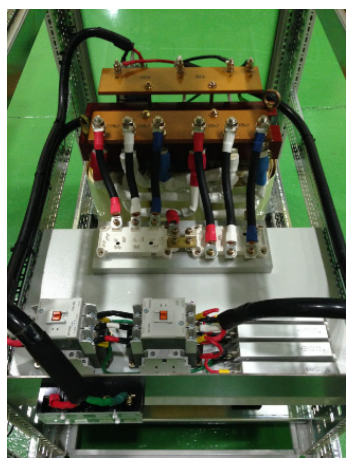

Figure 4: Input of the MPS configurations.

The power cover modules are configured as follows (Fig. 5). The topology of the MPS is applied to full-bridge inverter for bipolar current. The output stage is composed of a low-pass filter to reduce the switching harmonic noise. The LC filters have two stages in which the pole of first stage is a few kilohertz and second one is between switching frequency f_{sw}, and $f_{sw}/2$.

To simplify redesign to increase capacity, the power converters of the MPS are connected in parallel stages with common of DC link and load. Its power trains operate with a phase difference of 180°. The effective switching frequency at a magnet load is doubled. This configuration compactly reduces the hardware size of the MPS, and the switching pattern reduces current ripple.

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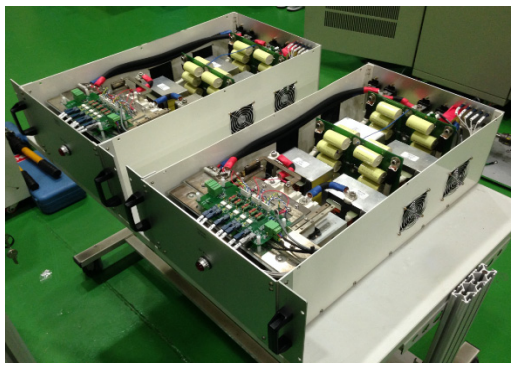

Figure 5: Power converter modules.

Experimental Results; Stability, Precision Control, and Repeatability

The current stability and precision were measured using a digital voltmeter (DVM3458A); the aperture time was set to 166.6 ms.

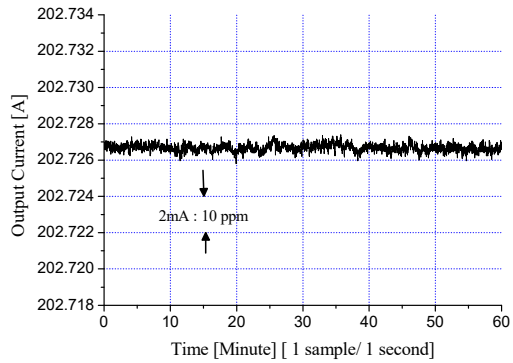

Figure 6: Measured output current stability using a proposed ADC scheme.

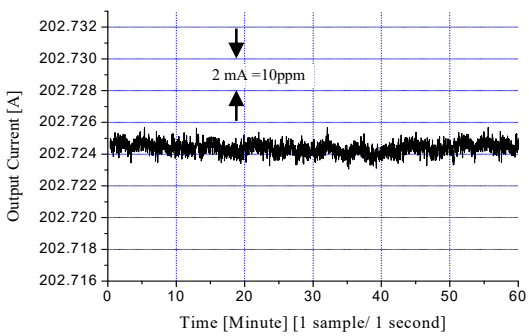

Figure 7: Measured output current stability using a single ADC chip of 16-bit.

Results obtained using the proposed ADC method are more stable than those obtained using a 16-bit single chip. The current was measured at 200 A; when the proposed ADC method was used, its variability was less than ~ 5 ppm (Fig. 6). When the output current stability using a single ADC chip of 16 bit was measured, the variability was ~ 10 ppm (Fig. 7). When 32-times oversampling was used, the developed AD circuit increased SNR by 18 dB and effective bit by 2.5 bit compared to an ADC chip alone.

The Fig. 6 and 7 show the measured precision and stability of the output current. When comparing the two results, the results obtained using a 16-bit single chip are less stable than those obtained with the proposed ADC method. The developed ADC method has better stability and precision than single chip method.

CONCLUTION

The proposed AD circuit is composed of parallel low-resolution ADC chips. Digital oversampling and aver-aging are performed to increase the resolution and SNR of the signal. A large amount of sampling data is averaged for each control period, so the resolution of the sampling data can be improved while greatly reducing the noise even in a noisy environment. The MPS that uses the developed ADC method provided a precise and stable current to the accelerator.

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