STATUS OF THE RF SYSTEMS FOR THE SPIRAL2 LINAC AT THE BEGINNING OF THE CONSTRUCTION PHASE

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Abstract

The Spiral 2 project [1] uses a RFQ and a superconducting linac to accelerate high intensity beams of deuterons and heavier ions. The accelerator frequency is 88 MHz. The construction phase was approved in Mai 2005 and the project organization was recently finalized. The RF Systems include power amplifiers and control electronics for the entire accelerator and some of the RF devices on the beam line: the slow and fast chopper and the rebunchers. The paper describes the status of the amplifiers prototypes, the architecture chosen for the digital LLRF and the preliminary studies on the other RF devices.

INTRODUCTION

According to the organisation of the accelerator division, the tasks of the *RF System* group include the supply of the power amplifiers and control electronics for the entire accelerator and of some of the RF devices on the beam line: the slow and fast chopper and the normal conducting rebunchers. All this equipment is schematised in figure 1, where the RFQ resonator and the cryomodules with the superconducting cavities are greyed as other groups are in charge of them.. Since the beginning, the SPIRAL 2 project is based on a large national and international collaboration. In the case of the RF systems, various laboratories already participate from the design to the commissioning of the different components: GANIL is in charge of the power amplifiers, the rebunchers and the fast chopper, CEA/DAPNIA of the control electronics, INFN/LNS is in charge of the slow chopper.

BEAM LINE DEVICES

The Slow Chopper

Requirements for the slow chopper have been established very recently and there are dominated by the ion beam dynamics with a bunch diameter of 62 mm. This figure leads to quite big plates whose geometry still has to be studied. Table 1 summarizes the main requirements.

Table 1: Slow chopper requirements

Deflecting voltage	± 5 kV
Deflecting length	160 mm
beam radial dimension (radius)	31 mm
Pulse length	100 us ÷ 1s
Pulse rise time	< 100 ns
Pulse repletion rate	> 20 Hz

The Beta 0.04 Rebunchers

The MEBT line, is equipped with 4 rebunchers whose parameters already include the future possibility to accelerate A/q=6 ions. The required voltage is 165 kV but, due to the high beam aperture, the Transit Time Factor (TTF) is quite low and a much higher voltage on the gap is required. To keep the longitudinal length of the cavity as small as possible, a 3 gap structure has been chosen.

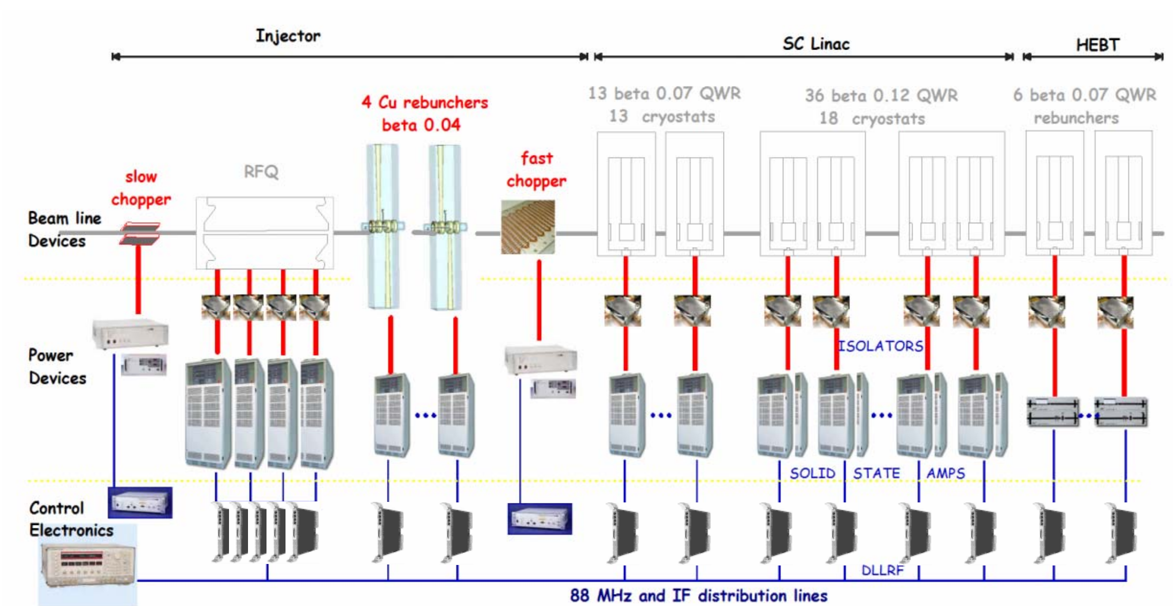

Figure 1: The RF Systems of the driver accelerator and of the high energy beam line.

The double quarter wave resonator of figure 1 is proposed instead of the classical split ring cavity. The stems can be manufactured and cooled more easily, and the gap geometry is better guaranteed. According to the preliminary thermal calculations, the displacement of the electrode can be kept below 0.2 mm. Thermal detuning will be compensated by a side plate with a stroke of 15 mm. The coupler is inductive and placed on the bottom of the cavity. The half height of the cavity is around 606 mm with a slight unbalance to compensate the presence of the coupling loop. Table 2 summarises the main parameters of the cavity.

Table 2: Parameters of the rebuncher cavity

Electrode voltage	102 kV
Beam aperture diameter	60 mm
TTF	0.39
Q	5600
Power consumption	11 kW
Max E field	10.2 MV/m
Max H field	9200 A/m
Flange to flange distance	300 mm

The Fast Chopper (Bunch Suppressor)

A fast chopper is required to isolate bunches and study the reaction issued by only one bunch on the target. The following parameters based on SNS values have been recently fixed but the feasibility has still to be studied, the frequency, the beta and the beam dimensions being significantly different.

Table 3: Requirements for the fast chopper

Deflecting voltage	± 2.5 kV
Deflecting length	450 mm
Deflecting section aperture	26 mm
Isolated bunch repetition rate	1:100 to 1:10000
Pulse rise/fall time	< 5 ns

POWER AMPLIFIERS

RFQ Amplifier

The last tests on the RFQ prototype have confirmed a Q factor about 10% lower than expected. Therefore, we can consider that the final cavity will require around 160 kW with a beam loading of few kW for ion operation voltages. Then, a total power of 200 kW has to be available at the amplifier. This power level is absolutely unusual at 88 MHz and we found only one manufacturer who could propose us a two stage tube amplifier, based on the TH 781 (250 kW) and TH 343 (20 kW) tetrodes, but whose cost is very high, being a single masterpiece. This considerations, associated to the parallel request from the RFQ group to drive the cavity keeping the four quadrant symmetry, lead to the scheme in figure 2. Four smaller amplifiers are coupled directly through the cavity, using four input ports placed at the same longitudinal position and one per quadrant to assure the polar symmetry. Four circulators are used to isolate the amplifiers and avoid oscillation problems. The I/Q modulators before the amplifiers compensate the gain and phase differences between the different branches. Four feedback slow loops could also be added if needed.

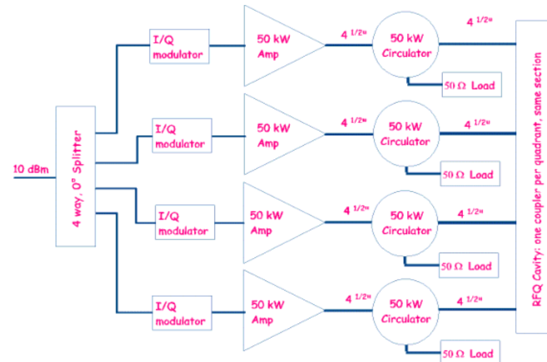

Figure 2: 4 Amps plus circulators scheme.

Standard FM amplifiers are much less expensive but limited to 30 kW. Only one triode is used, the first stage being solid state. A 40 kW prototype, based on the same technology but using a more powerful tube (3CW 40000) was bought for the coupler test bench but it appeared to be unreliable when used at maximum power. Considering the encouraging results recently obtained with solid state modules at SOLEIL [2], we are still studying whether a solid state solution couldn't be more interesting both on the cost and the reliability aspects.

Solid State Amplifiers

10 and 20 kW units are required for the 2 families of the SC linac. The FM technology has strongly progressed these last years and standard solid state amplifiers are now available at this power level. Water cooling has been required with respect to the standard FM technology, to simplify the maintenance of the cooling equipment, to increase the Mean Time Between Failure (MTBF). Each amplifier is equipped with an external circulator and dummy load to sustain mismatched operating conditions. This solution was preferred to the use of distributed circulators at the output of the transistors as it is less expensive, sustains higher SWVR and protects the combiners and the transmission lines too. The first prototypes of the amplifiers and of the circulators should be ready by the end of the year.

A 20 kW test bench able to produce all SWVR conditions has being studied and is being assembled at Ganil and will be used for the amplifiers and circulators commissioning, the first prototypes of which should be delivered by the end of the year.

LLRF

General Architecture

Since the beginning, a digital LLRF (DLLRF) has been chosen because of the advantages in terms of flexibility, diagnostic and maintenance such a system can offer, with respect to the analogic solution.

Flexibility of the control loops is required by the different type of cavities the system has to deal with: normal and superconducting, accelerating or bunching ones. Large differences exist also in the tuning systems and in the conditioning procedure against multipacting. Moreover, the long term operation and maintenance of the facility require the possibility to adapt the RF control electronics during the commissioning of new beam intensities, energies, pulse lengths or other beam characteristics. Diagnostic possibilities are recognised as some of the most efficient factors to reduce the time required for trouble shouting and thus to increase the accelerator availability. The DLLRF will include a data buffer to facilitate this trouble shouting (see below).

From the digital choice for the LLRF, we expect electronics boards to be the same for all the cavities, implementing different and adaptable filters or signal processing algorithms as required by each type of cavity.

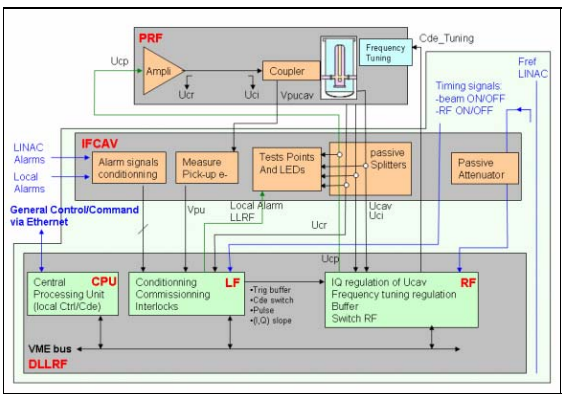

Figure 3: The LLRF architecture. The LLRF subsystems, in the green box in the figure, include (1) Generation and distribution of the reference frequency and of the timing signals; (2) Digital processing electronic boards (DLLRF) and (3) Physical Interfaces between the various RF cavities and the DLLRF.

Figure 3 shows the architecture of the LLRF: The complete LLRF system includes the central generation of the reference frequency and of the timing signals, their distribution in the whole facility, the DLLRF, and physical interface panels named “IFCAV” on Figure

The interface panels provide mostly connecting interfaces, test points and allow having a common DLLRF hardware for all types of cavities. They hold passive components, LED-based displays and the measurement units of the power coupler multipactor.

At the bottom part of figure 4, the DLLRF schematics are displayed. A full custom Versa Module Eurocard (VME) electronic design has been preferred to the assembly of commercial-off-the-shelf modules to obtain a more compact hardware and to make the maintainability easier.

The DLLRF includes:

- A central processing unit (CPU), which will be a commercial VME board, communicating with the upper level control-command via Ethernet.
- A ‘Low Frequency module’, which is responsible for the processing of the various alarms, and for the automated conditioning of the cavity (for this task, the CPU will dialog with the vacuum controller and write adequate parameters in the FPGA registers).
- A “Radio Frequency” module, which is responsible for the rapid IQ regulation of one RF voltage, and of the frequency tuning regulation of one cavity. This module also holds a FIFO-like memory buffer, which stores all the digital data concerning the regulations during 1-2 minutes with a time resolution of 100 ns or better, to serve as a diagnostic tool in case of an alarm trigger.

A single custom-made VME64X board (possibly with the addition of a rear-IO module) should be able to hold the two last modules, thus all the necessary electronics to control one cavity; for the specific case of the Radio Frequency Quadrupole (RFQ), four more boards could be used to control the amplifiers. For the 42 cavities of the accelerator, the complete DLLRF system will consist of up to 8 VME racks equipped with such VME boards, distributed along the accelerator.

RF Module

The RF module is the heart of the DLLRF system. Given the relatively low operating frequency of 88 MHz of the Spiral-2 RF cavities, the digital IQ demodulation of the cavity RF signal can in principle be done by direct sampling of the RF voltage, for example at 4/5 of the RF frequency (i.e. 70.4 MSample/s). This solution is attractive, compared to the traditional IF frequency operation, because it requires less RF components. It will be evaluated during a detailed study phase, before freezing the sampling technique.

The regulations loops of both the RF field and the frequency tuning will be implemented in a Field Programmable Gate Array (FPGA), the set points being defined as registers accessible via the VME controller. The present assumptions for the regulation requirements of each RF field are ±1° in phase, and ± 1% in amplitude.

The feed-forward functionality, if required, will also be implemented in the FPGA.

Finally, it will be possible to change the FPGA loop parameters, locally or remotely, via the JTAG boundary scan mechanism. More generally, it will be possible to fully re-configure the FPGA responsible for the IQ regulation computations, using this mechanism.

REFERENCES

[1] T. Junquera et al., Proc. of EPAC 06, p.1559
[2] T. Ruan et al., Proc. of PAC 05, p. 811