# FPGA BASED DIGITAL RF CONTROL FOR FLASH

Przemyslaw Fafara, Wojciech Jalmuzna, Waldemar Koprek, Karol Perkuszewski, Krzysztof Pozniak, Piotr Pucyk, Ryszard Romaniuk - Warsaw University of Technology

Stefan Simrock - DESY

*Abstract*

This article summarizes FPGA based systems which have been installed recently at FLASH facility at DESY. Main concept of the control algorithms is presented and the description of the SIMCON 3.1 board used for this purpose is shown. Moreover some plan for the nearest future are introduced including distributed control system concept.

## INTRODUCTION

The currently operating LLRF system at FLASH is based on the C67 DSP processor to process the control algorithm. The controller is divided into three boards – 1MHz ADC board, processing board and DAC board. All the boards are connected to one another using gigalink interface. Actual computation power of the system is close to the limit. Loop dealy including klystron and the cables is of the order of 4us. The only way to extend the feedback algorithm with new features was to add more DSP processors. This solution requires integration of new DSP board into existing system. It may cause some additional problems and delays in the machine operations.

During past years very fast progress on the FPGA market was observed. Nowadays FPGA chips have reached the computation power that can be compared with DSP processors, but can be achieved with lower latency. The architecture of those chips is not fixed. Just like software algorithms it can be optimized to achieve required speed or resources usage. FPGA chips offer variety of the embedded solutions such as PowerPC, Microblaze, Nios which can be easily used in addition to fast, parallel signal processing. Moreover large number of user pins makes it possible to integrate all the elements necessary for the control into one PCB board. Therefore for evaluation purposes some parts of the system were replaced by FPGA based boards. This poster summarizes the FPGA boards that are currently in use and describes algorithms executed by these boards.

## SIMCON 3.1 BOARD

SIMCON 3.1 board is the multi-purpose FPGA based board equipped with 10 ADCs, 4 DACs, external SRAM and SDRAM memory and multiple IO interfaces such as VME, RS232, Ethernet. Computation power of the Virtex 2 Pro chip exceeds the computation power of the DSP processors used in the current FLASH control system. That is why this board is used as an universal development platform for the LLRF system. During last 6 months rf controls for the RF-GUN and first cryomodule have been implemented with this board and left for permanent operations

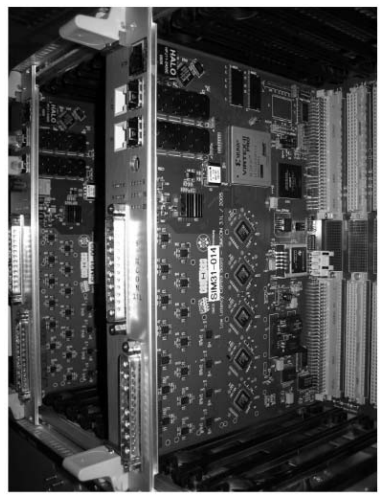

Figure 1: Simcon 3.1 board.

## RF-GUN CONTROLLER

DSP based RF-GUN field control used previously was only able to stabilize the RF output of the klystron. This was due to the lack of processing power and the overall loop delay. The controller was not able to provide satisfactory rf field stability in the gun. Replacing the DSP hardware by the new FPGA-based hardware, we are able to reduce the latency within the digital part significantly allowing for higher loop gain. The control algorithm is described below.

From the set point table, a 1.3 GHz drive signal is generated via a digital to analog converter (DAC) steering a vector modulator. This signal is amplified by a preamplifier and a klystron generating up to 3 MW of rf power driving the gun via an axial symmetric input coupler. The rf field inside the cavity is determined by the forward and reflected power measured at a directional coupler. Both directional coupler signals are down converted to the baseband and sampled by ADCs. After signal calibration, the controller calculates the vector sum providing a ‘virtual rf probe’ signal for the subsequent control algorithms. Subtracting the ‘probe’ signal from the set point gives the error signal.

Amplifying slow varying error signals by the gain factor g and adding the result to the drive signal reduces

the field error by 1/(1+g). For error signals changing faster than the time required for the signal to propagate through this (fast) proportional control loop (1), we get positive feedback and the loop becomes unstable for higher gain factors. High frequency error signals are suppressed by the 60 kHz bandwidth of the gun copper cavity. Together with the loop delay of 1.3 μs this results in a maximum stable gain of about 3.

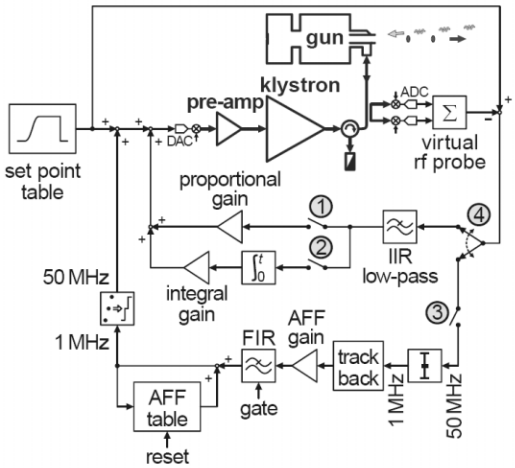


Figure 2: RF-GUN control algorithm.

## ACC1 MODULE CONTROLLER

The DSP system used in the ACC1 module did not allow to add more required features. Switching to the FPGA controller decreased the overall latency and increased possible loop gain by the factor of 2. Moreover features as beam load compensation ( using toroid signal ) and adaptive feedforward ( AFF ) were implemented on board. The control algorithm performed by the controller is described below.

The main control loop in the LLRF system starts at the cavity probe. The signals (1.3GHz) are downconverted to an intermediate frequency of 250KHz. Eight downconverted signals are connected to inputs of digital controller. It samples the probe signal with a frequency of 1MHz. Inside the controller (currently it is a DSP based system) after initial calibration (scaling and levelling), the digital processing is performed in I/Q detector applying the signal v_m of the intermediate frequency at 250 kHz. The resultant cavity voltage envelope (I, Q) is calibrated, so to compensate the phase offset for an individual measurement channel. The vector sum of up to 32 signals is needed for the actual control processing. Feedforward and Feedback algorithms can be used to control the system.

The Set-Point table delivers the required signal level, which is compared to the actual average value of the cavities voltage envelope. Then the proportional controller amplifies the signal error according to data from the GAIN table and closes the feedback loop. Additionally the Feed-Forward Table is applied to improve compensation of the repetitive perturbations induced by the beam loading and by the dynamic Lorentz force detuning. I and Q signals are produced to drive the klystron. These two signals are used by the vector modulator to reconstruct the complex signal. The output of this vector modulator drives the klystron.

Additional algorithms such as Adaptive Feedforward are performed by embedded PowerPC processor.

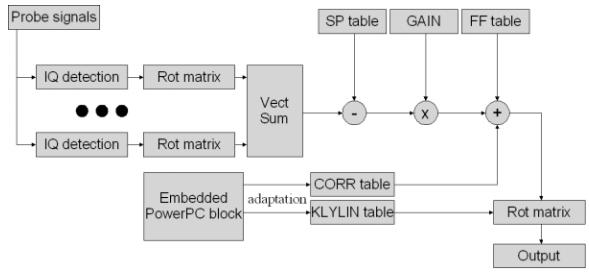


Figure 3: ACC1 control algorithm.

## CONTROL SOFTWARE

To integrate described modules into working system, the DOOCS framework had to be used. Therefore dedicated DOOCS servers and GUI interfaces were developed. DOOCS server for SIMCON have to read and process 320kB of data (40 internal diagnostic and control signals) every 200ms. To provide such efficiency DMA (Direct Memory Access) and interrupts have been used. To avoid server overloading, system consists of two separate applications. First reads data from SIMCON memory and the second one presents data to the user. Communication between them is based on shared memory.

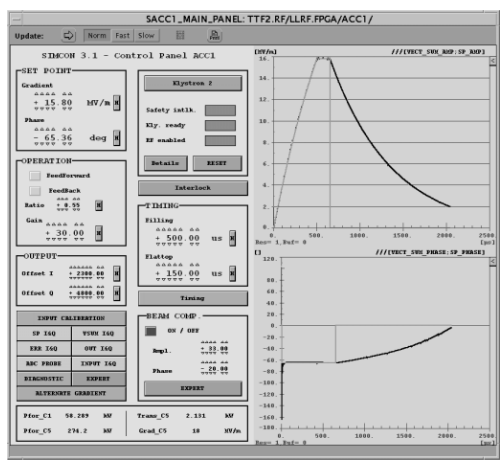


Figure 4: ACC1 DOOCS control panel.

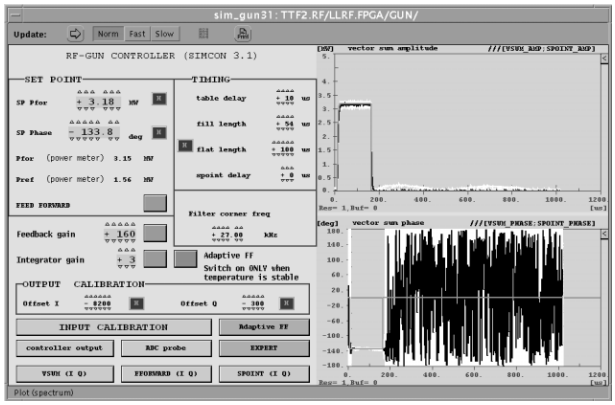


Figure 5: RF-GUN DOOCS control panel.

## FUTURE PLANS

In the near future the next generation of the SIMCON board will be available. The main advantage is a DSP processor on-board. It will be use to perform some pulse-to-pulse algorithms. The next task is to distribute algorithms to the available processors. This will decrease overall load of the control applications and further reduce latency of the control process.

Algorithm and controller structure described for ACC1 module will become the base for the Universal Controller presently under development.

Moreover distributed control system solutions will be tested using FPGA based gigalink concentrator.

## REFERENCES

[1] W. Giergusiewicz, W. Jalmuzna, K. Pozniak, N. Ignashin, M. Grecki D.V.M., D. Makowski, T. Jezynski, K. Perkuszewski, K. Czuba, S. Simrock,R. Romaniuk, 'Low latency control board for LLRF system – SIMCON 3.1.', Proc. of SPIE Vol. 5948, 2005

[2] Elmar Vogel, Waldemar Koprek, Piotr Pucyk 'FPGA based rf field control at the photo cathode rf gun of the DESY vacuum ultraviolet free electron laser'

[3] Krzysztof T.Pozniak, Ryszard S.Romaniuk, Wojciech Jalmuzna, Krzysztof Olowski, Karol Perkuszewski, Jerzy Zielinski, Krzysztof Kierzkowski 'FPGA Based, Full-Duplex, Multi-Channel, Multi-Gigabit, Optical, Synchronous Data Transceiver for TESLA Technology LLRF Control System' – TESLA Reports 2005

[4] Wojciech Giergusiewicz, Waldemar Koprek, Wojciech Jalmuzna, Krzysztof T. Pozniak, Ryszard S. Romaniuk 'FPGA Based, DSP Integrated, 8-Channel SIMCON, ver. 3.0. Initial Results for 8-Channel Algorithm' – TESLA Reports 2005

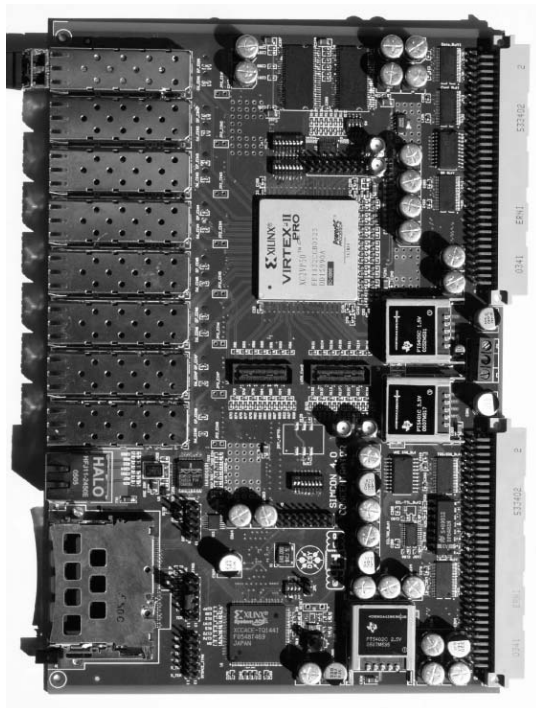


Figure 6: SIMCON 4.0 concentrator board.