FREQUENCY SOURCE FOR THE ISAC RFQ

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Abstract

The ISAC RFQ cavity nominally operates at a frequency of 35 MHz. It can operate in either self-excited or driven mode. In the self-excited mode, the RFQ cavity itself is one of the frequency-determining elements. In the driven mode, the frequency is slaved to an external stabilized, digitally synthesized frequency source. In order to achieve glitchless transitions between the two modes, the RFQ frequency source is buffered by a phase-locked loop. When operating in the driven mode, RF switches in the loop configure the loop to lock to the external direct digital synthesizer. Reconfiguration of the RF switches in the self-excited mode turns the phase-locked loop into an oscillator whose frequency is determined by the phase shift of the RFQ cavity. The overdamping characteristic of the phase-locked loop prevents sudden transitions in either frequency or phase during switching between operating modes.

1 INTRODUCTION

The ISAC RFQ accelerator is a high Q, 4-rod RFQ with a peak potential between the electrodes of 74 kV. When operating under the fixed frequency mode, a stabilized direct digital synthesizer, whose frequency can be controlled remotely, drives the RFQ. During the powering and warming up phase, before the RFQ cavity reaches its operating temperature, the preferable mode is the self-excited mode, where the rf frequency is slaved to the resonance frequency of the RFQ cavity. The rf control system must be able to switch between these two modes under full power. Since the DDS frequency and the self-excited frequency are often different in frequency as well as in phase, this switching must be performed in such a way that will result in a gradual phase transition to prevent overloading the final RF power amplifier. A rf switch is used to provide the frequency switching, while a phase-lock loop is used to buffer the resultant switching transition. The phase-lock loop is designed with a large overdamp factor to enable the RFQ rf system to switch from one mode to another without generating large phase excursion.

2 DIRECT DIGITAL SYNTHESIZER

For operation of the RFQ in the driven mode, a frequency source whose output frequency ranges from 35.654517MHz to 35.851119MHz is needed. A digital direct synthesizer (DDS) is used to provide a very stable source with fine resolution, and is able to change frequency without generating phase jumps. As shown in Figure 1, a DDS is used as the core of this frequency source.

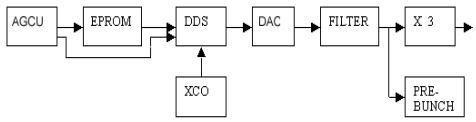

Figure 1: Block diagram of DDS

The phase data, which is stored in the EPROM shown in Figure 1, and the clock frequency are directly related to the output frequency by the equation (1).

$$f_o = \frac{f_c x(-\,phase)}{2^{32}} \qquad (1)$$

where f_c is clock frequency generated by an 80 MHz crystal oscillator (XCO), *-phase* is the phase data. The DDS input phase resolution is 32 bit, but the phase bus between the DDS and the EPROM is only 8 bit. Therefore, it is necessary to transfer the phase data four times from the EPROM to the DDS to obtain a new frequency. This control logic is performed by the Address Generator Control Unit(AGCU).

The DDS output frequency is the third sub-harmonics of the RFQ frequency (i.e. 11.884839MHz to 11.950373MHz). The DAC is used to convert the frequency digital data to analog voltages. A 3-pole Butterworth bandpass filter removes any spurious frequency components and splits the signal into two paths: one is used as the frequency source for a buncher placed upstream the RFQ and another requires tripling the frequency in order to obtain the desired frequency for the RFQ. The design frequency resolution is 6Hz and its stability is better than 1ppm.

3 PHASE-LOCK LOOP

The RFQ can be operated either under the driven mode, in which the DDS is used as the master frequency source, or in the self-excited mode, in which the signal from the RFQ cavity is used to determine the excitation frequency. An internally terminated high-isolation rf switch is used to select between the two frequency references. A phase-lock loop (PLL), with its versatility in frequency control, acquisition times, and step response, is used as a buffer

after this mode selection switch. A low phase drift limiting amplifier with 30-dB dynamic range is placed between the switch and the PLL to eliminate the amplitude dependency of the circuitry. The performance requirements of this RFQ PLL are different from that of an ordinary frequency synthesizer. In particular, it is designed to have a slow step response in order to satisfy the following two requirements.

1. The ability to switch from self-excited to driven operations under full power without phase jumps.
2. The ability of the entire system to recover from sparking in a rf cavity.

A spark can collapse the rf field in the cavity. Sometimes within several microseconds the RFQ voltage may recover after the spark has dissipated. The inclusion of the PLL circuitry is designed to be highly overdamped such that its VCO frequency does not react to the disturbance during this time interval. The power amplifier keeps energizing the cavity with rf power at the last resonance frequency allowing the cavity field to recover. The transfer function of the PLL is given by

$$\frac{\theta_o}{\theta_i} = \frac{G}{1+GH} \tag{2}$$

with

$$G = \frac{K_v K_p F}{s} \tag{3}$$

and

$$H = 1.$$

In equation (2), θ_i is the phase at the input of the PLL, and θ_o is the phase at the output of the PLL. In equation (3), K_V is the VCO sensitivity, K_p is the phase-detector gain constant, and F is the transfer function of the filter. Together they determine the response characteristics of the PLL. A unity gain bandwidth in the order of kHz and a phase margin of more than 45^o provides enough damping for spark recovery. Using a type 2, second-order PLL, zero frequency error at dc is guaranteed. The schematic of the PLL filter is shown in Figure 2.

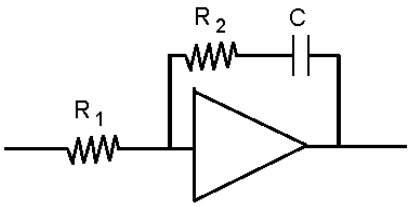

Figure 2: Schematic of PLL integrator/filter

In equation (3), the filter transfer function, F, is given by

$$F = -\frac{1+sT_2}{sT_1} \tag{4}$$

where $T_1 = R_1 C$ and $T_2 = R_2 C$. Figure 3 shows the output spectrum of the PLL. The x-axis shows the frequency at 5 kHz/div. The y-axis shows the power at 10 dB/div. This spectrum displays typical noise distribution of PLL output. The background noise is -70 dBc, while the oscillator noise with a bandwidth of 20 kHz is –55 dBc.

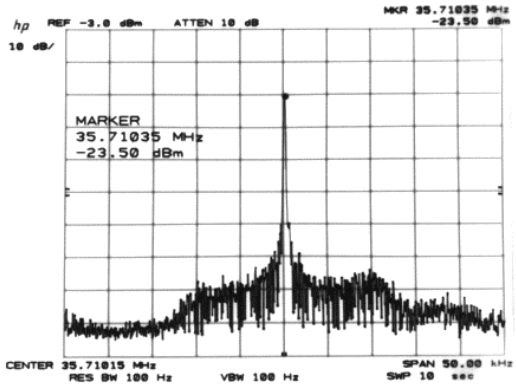

Figure 3: Output spectrum of PLL

4 SELF-EXCITED OSCILLATION

In the self-excited mode, the RFQ cavity determines the rf frequency. This is achieved by feeding the signal voltage at the RFQ cavity back into the input of the PLL. Thus θ_i is given by

$$\theta_i = \theta_o + \Delta\theta_m + \Delta\theta_l + \theta_c \tag{5}$$

where $\Delta\theta_m$ is the phase shift from the VCO to the output of the vector modulator. $\Delta\theta_m$ is the sum of the phase delay due to the VCO to the modulator and the phase shift of the vector modulator. $\Delta\theta_l$ is the phase shift due to the transport lag of the feedback loop. θ_c is the phase shift caused by the RFQ cavity. When the excitation frequency ω is close to the resonance frequency ω_o of the cavity,

$$\theta_c = -\frac{2(\omega - \omega_o)}{\omega_o} Q \tag{6}$$

Q is the quality factor of the cavity. These phase shifts must be adjusted to satisfy several constraints. In order to reduce crosstalks between channels in I/Q feedback loops, it is necessary to set the phase shift from the vector modulator to the vector demodulator to be integer multiples of 360^o (i.e. $\Delta\theta_l + \theta_c \cong 0.$). For proper operation of the self-excited mode, the phase shift from the output of the VCO to its input should also be integer multiples of 360^o. As a result, $\Delta\theta_m + \Delta\theta_l = 0$. This also implies that for the Q channel, the regulation is disabled and the open loop drive is set to zero. The overall phase relationship is illustrated in Figure 4.

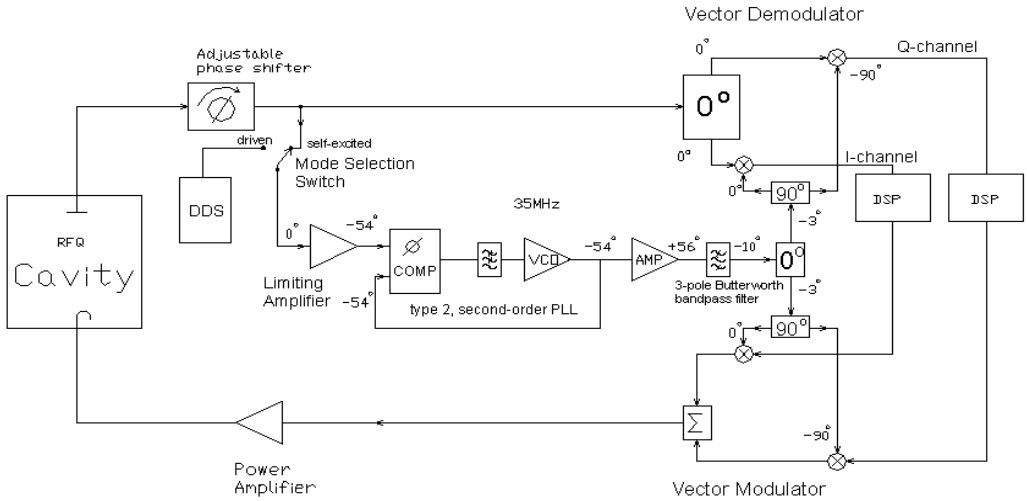

Figure 4: Phase relationship for proper operation of self-excited oscillation

When the above conditions are satisfied, the PLL will oscillate at

$$\omega = \frac{1+sT_2}{1+s\left(\frac{T_1\omega_o}{2K_pK_vQ}+T_2\right)}\omega_o \qquad (7)$$

The PLL in the ISAC RFQ has the following parameter values:

$$T_1 = 330\mu s$$
$$T_2 = 50\mu s$$
$$K_p = 0.16V/rad$$
$$K_v = 500\times10^3\ rad/s/V$$
$$\omega_o = 35.75\times10^6\cdot 2\pi\ rad/s$$

With these parameter values, Equation 7 then reduces to

$$\omega = \frac{1+\frac{s}{3\times10^3}}{1+\frac{s}{9\times10^3}}\omega_o \qquad (8)$$

where ω_o, the resonance frequency of the cavity, is the only varying factor. Since the variation in ω_o is due to thermal expansion, it varies slowly and thus,

$$\omega \cong \omega_o$$

Thus, the PLL tracks the resonance frequency of the RFQ cavity.

All the above mentioned circuitries (i.e. the PLL, the mode selection switch, the limiting amplifier, the vector modulator and the vector demodulator) are placed into a single C-size VXI module. In operation, the low pass filter at the PLL output is adjusted to give the desired phase shift as shown in Figure 4. Final phase adjustment is carried out using the variable phase shifter after the cavity. During self-excited mode operation, the Q-channel is disabled and the phase shifter is adjusted for minimum VSWR.

5 SUMMARY

The mixing of digital and analog technology in the frequency source for the RFQ allows for both performance and flexibility. A direct digital synthesizer is able to generate a highly stable and programmable frequency source. An overdamped phase-lock loop allows the rf power amplifier to switch from a self-excited mode to a driven mode without sudden phase jumps. To date, the system has been running in close-loop operation with the ISAC RFQ cavity. Stable operation has been achieved with both self-excited and driven modes. Switching between the two modes has been demonstrated at different power levels including full power without tripping the rf power amplifier. Spark recoveries at both modes are also observed to be similar. The rf system is able to recover from short duration sparks. In the driven mode, the digital direct synthesizer (DDS) as a frequency source is capable of reaching high stability, high resolution and is proving to be easily controlled.

REFERENCE

[1] M. Laverty, K. Fong, and S. Fang, "A DSP-based Control System for the ISAC Pre-Buncher," International Conference on Accelerator and Large Experiment Physics Control System, Beijing, Nov. 1997