LEDA LLRF CONTROL SYSTEM CHARACTERIZATION*

A.H. Regan
Los Alamos National Laboratory, Los Alamos, NM 87545
P. Balleyguier
Commissariat a l'Energie Atomique, Bruyeres-le-Chatel, France
C.D. Ziomek
ZTEC, Inc., Albuquerque, NM 87109

Abstract

The Low Energy Demonstration Accelerator (LEDA) for the Accelerator for the Production of Tritium (APT) project will be built at Los Alamos National Laboratory. The low-level RF (LLRF) control system portion of this accelerator must perform many functions, of which the primary one is controlling the RF fields in the accelerating cavities. Plans have been made to provide for on-line characterization of the LLRF control system and the complete RF system through use of stimulus and response buffers, and a digital signal processor built into the field control system electronics. The purpose of this circuitry is to characterize the behavior of the entire RF system (klystron, waveguides, high power splitters, accelerator cavity, etc.). This characterization feature can be used to measure the performance of the closed loop system with respect to the open loop system, to provide an automated way to set loop parameters, to determine the cavity Q-curve, and to detect any abnormal behavior in the RF chain. The types of measurements include frequency and time-domain responses to given perturbations, amplitude modulations, etc. This paper will discuss types of algorithms that can be implemented and present a description and block diagram of the electronics to be used.

1 BACKGROUND MOTIVATION

Initially LEDA will be operated "manually" as we bring systems on-line individually. However, in planning for the APT plant, it is realized that we will be operating an accelerator with upwards of fifty control systems. Automatic calibration and test sequences will enable the operators to quickly diagnose a system and anticipate possible failures. In addition, performing a dynamic frequency response measurement of the RF chain around its normal working point, will provide for characterization of individual control systems throughout their "lifetime."

Here the RF chain refers to part of the LLRF control system hardware, the preamplifier, the klystron, waveguide, high power splitters, couplers, cavity, pickup loop, downconverter, and return signal cable. This measurement will be a special mode of operation, incompatible with the normal control algorithm. The aim is to measure how a known perturbation at a given frequency is transmitted along the RF chain.

Uses of such measurements include:

- Optimizing performances of the control system, by predicting ultimate loop gain possibilities
- Checking performance of closed loop operation with respect to open loop
- Setting the correct loop phase shift
- Detecting any abnormal behavior in the RF chain

2 DISCUSSION

One of the primary functions of the low-level RF control system is to maintain the field levels inside the accelerating cavities. The basic VXIbus module architecture for the LEDA LLRF control system has been described previously[1] as well as some preliminary low-level RF modeling for the APT[2]. By implementing a LLRF control system that provides easy software/hardware interaction, other functions can be implemented besides simple real-time setup by the accelerator operators. Software can also be used to perform RF system analysis.

A fundamental component of the LLRF control system is the Field Control Module (FCM). This module is a feedback/feedforward controller used to regulate the RF field parameters of the accelerator cavity. The FCM performs cavity field feedback and beam feedforward control algorithms in both digital and analog circuitry. The digital processing on the FCM is centered around a Texas Instruments TMS320C50 fixed point digital signal processor (DSP). The DSP processor provides powerful control algorithms and flexible operational scenarios. The digital processing provides precision detection and flexible control signals to bandwidths around 10 kHz. In order to extend the bandwidth beyond this, analog circuitry is used to process the field and beam signals in parallel with the DSP. The analog circuitry is more susceptible to errors and noise, and is less flexible, but provides control signal bandwidths to around 1 MHz. A block diagram of the FCM is depicted in figure 1.

The flexibility of the digital processing on the FCM is demonstrated by its ability to function in significantly different operating modes. The operating modes encompass many different operational scenarios including continuous operation, pulsed operation, amplitude modulation, phase modulation, frequency modulation, amplitude and phase control, amplitude-only control, open-loop operation, and closed-loop operation. Also, setpoints, gains, bandwidths, and algorithms can be adjusted by the operator through the VXIbus interface. In

addition to the control circuitry, the FCM includes circuitry that performs self-calibration and system characterization. The calibration and characterization functions are accomplished with either frequency modulation or arbitrary waveform modulation.

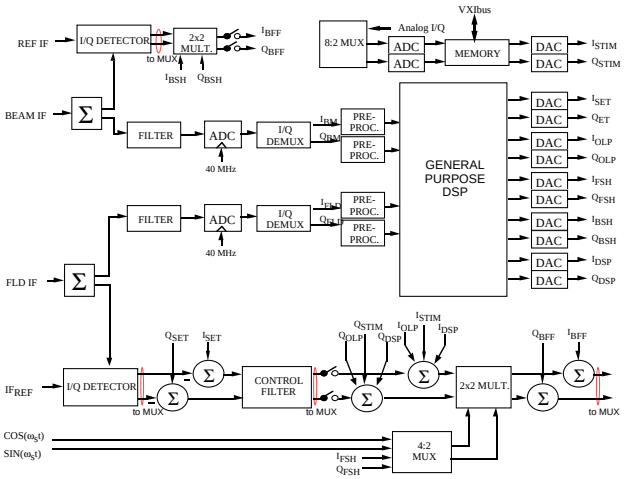

Figure 1. Block Diagram of Field Control Module

The frequency modulation functionality can be used for self-calibration of the in-phase/quadrature (I/Q) detectors on the FCM and other modules in the system. The FCM can be placed into an operating mode where it generates a control output that applies a frequency shift to the master oscillator frequency. The original purpose of this shift is to provide a means of resonance tracking to rapidly heat the accelerating structure after a RF fault.[3] It has the additional feature though, of providing us with a means of inputting a test frequency for measurement of the offsets, quadrature errors, and gain imbalances in the I/Q detectors. This frequency modulation functionality will also allow us to modulate the klystron drive with a swept FM signal, something SLAC has found quite useful for processing cavities.

The arbitrary waveform modulation functionality can be used to characterize the RF system response and configure the RF system control parameters. The arbitrary waveform functionality is provided by stimulus and response waveform buffers on the FCM. The stimulus waveform buffer allows loop excitation with arbitrary modulation signals stored in memory and converted to analog signals in DACs operating at 10 MHz. The response waveform buffer captures the response of the RF system to the stimulus. Various points along the signal path in the FCM can be multiplexed and their data stored for later analysis. The cavity field feedback signal can be examined to characterize and configure the total RF system. In effect, this can be thought of as a baseband arbitrary waveform generator, with the ability to perform baseband network analysis.

The first step to system characterization is to set the DSP outputs to a constant value such that the normal field level is measured in the cavity (without beam). A generated perturbation (test signal) is then added to the normal output values to generate the perturbed input signal (I_{STIM} and Q_{STIM}). We will operate the klystrons some percentage below saturation, in order to allow operating room for the disturbance input. The modulation we place on the drive will be simply some small noise on top of a baseband level. One type of test signal consists of a succession of pre-calculated samples at a certain frequency rate and during a certain period of time. While this test signal is being injected into the system, the cavity field perturbed inputs to the DSP are measured and stored for future analysis. Therefore, the only real-time process would be to read a pre-calculated complex signal, add it to a constant value, output this signal at a certain frequency rate, acquire the perturbed signal at the same frequency rate, subtract the constant value, and store it in memory. All other analysis could be done after this sequence, in a non-real time mode by the supervisory system software, EPICS.

Some of the input test signals will be time domain versions of single frequency tones at known system-problem frequencies. Other possible input test signals include chirp pulse-compression waveforms. This methodology will also allow us to modulate the RF drive with a swept frequency signal for frequency-domain analysis of the RF system. In another test scenario, a small amount of white noise can be injected. Such a technique has been used with success on the ELSA linac at Bruyeres le Chatel.[4] The test signal was actually a special kind of noise: constant in amplitude and random in phase in the frequency domain. We anticipate bandwidth-limiting the noise for better measurements, and more realistic inputs.

Off-line processes include generating the desired input test signals and performing data analysis. One nice feature about EPICS is its ability to incorporate MATLAB functions. MATLAB, a control system design and analysis software package, has a very useful function known as TFE. The Transfer Function Estimate simply requires a set of system inputs and outputs, for which it returns the system's transfer function. The complex frequency response can then be plotted in the complex plane with frequency as a parameter, or as a Bode diagram. Once transfer functions are calculated, they can be compared to models for determining desirable operating parameters

3 HARDWARE SPECIFICS

A photograph of the Field Control VXIbus Module is shown in figure 2. The analog electronics are along the bottom of the module, while the digital hardware is located in the upper two thirds. The analog circuitry consists of two intermediate frequency I/Q detectors, baseband analog PID control circuitry, analog switches and multipliers for adjustments, and the analog control

output drivers. The digital circuitry consists of quadrature-sampling ADCs, decimating digital filters, the DSP, the control output DACs, the DSP memory resources, and the VXIbus interface. In addition, The FCM contains the stimulus waveform memory banks and DACs and response waveform memory banks and ADCs.

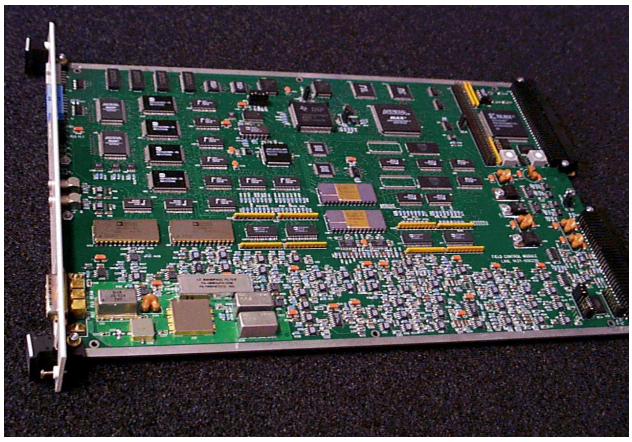

Figure 2. Field Control VXIbus Module

The EPICS interface to the stimulus/response functionality is accomplished with two sets of read/write registers that have been designated as the Stimulus I (or Q) Memory Register and the Response I (or Q) Memory Register. These registers provide access to the First-In, Last-Out (FILO) memory buffers for the stimulus DACs and response ADCs. Each FILO memory is 256 kwords in length, providing a time duration of approximately 26 ms at the 10 MHz DAC and ADC rate. In order to measure the response of the system, the FILO memory buffers are placed in their record mode, thus capturing response waveforms from the control system. There are two possibilities for the time-duration of the stimulus/response signals. The continuous duration causes the stimulus waveforms to be generated repeatedly and the response waveforms to be captured repeatedly. The single duration causes the stimulus DACs and response ADCs to generate and capture data only once until the waveform buffers are full. After the response waveform buffers are full, the FILO memory buffers stop and the VXIbus host processor is notified.

4 CONCLUSION

The FCM is one of five fundamental modules in the APT LEDA LLRF control system. It not only performs analog and digital field control, but has some features built in to allow us to perform on-line RF system characterization. This will be useful in determining various operational parameters, as well as provide a means for conditioning cavities. We expect to integrate the first LLRF control system with the rest of LEDA later this year. Once commissioning commences, one of the first LLRF tests we will perform is RF system characterization.

REFERENCES

[1] Regan, A.H., et al, APT LLRF Control System Functionality and Architecture," Proceedings of Linear Accelerator Conference 1996, Geneva, Switzerland, August, 1996, pp. 225-227.

[2] Regan, A.H., Ziomek, C.D., "APT LLRF Control System Model Results," Proceedings of PAC '97, Vancouver, Canada, May 1997.

[3] Rees, D.E., et al, "Design and Test Results Of The Low Energy Demonstration Accelerator (LEDA) RF Systems, " Proceedings of EPAC '98, Stockholm, Sweden, June, 1998.

[4] Balleyguier, P. "Pulsed Network Analysis with Random Signal for RF Feedback Optimization," IEEE Trans. Nucl. Sci., Vol. 43, No. 4, August 1996, pp. 2337-2342.