

PCI to VME interface

SIS1100/3100 Short Description

The SIS1100/SIS3100 PCI to VME interface card combination was developed to meet the requirements of demanding VME data acquisition systems. The link is optimised for low latency high speed readout. Interaction with external logic is possible through input/output connectors on the VME side (SIS3100) of the link. The actual VME transactions are handled by a sequencer. The sequencer can execute stored command lists from the sequencer RAM or asynchronous commands from the sequencer FIFO. The sequencer command set comprises wait for external input and set output, what allows interaction with user deadtime logic.

The flexible FPGA based design allows for the implementation of the traditional VME cycles as well as more recent extensions to the standard, like 2e MBLT64 e.g.

Functionality

VME Side

- VME List sequencer
- Sequencer RAM and FIFO
- Mapping table with 128 entries
- VME master A16/A24/A32/A40 D8/D16/D32/
BLT32/MBLT64/2eMBLT64
- VME slave A32/D32/BLT32/MBLT64
- Block transfer address auto increment on/off (for
FIFO reads)
- System controller function (can be disabled by
jumper)
- Gigabit link medium (optical)
- 2 - 450 m link distance

Options:

I/O Option

- I/O FPGA
- Connectors for SIS9200 DSP
- DIMM socket
- 3 LEMO inputs (NIM or TTL)
- 3 LEMO outputs (NIM or TTL)
- LEMO reset input (NIM or TTL)
- LEMO reset output (NIM or TTL)
- 4 flat cable outputs (ECL or TTL)
- 4 flat cable inputs (ECL or TTL)

DRAM Option (in conjunction with I/O option only)

- DRAM controller
- 64, 128, 256 or 1024 MB slave/histogramming
memory

DSP Option (in conjunction with I/O option only)

- SIS2900 SHARC DSP piggy

Long Distance Option

- Mono mode transceivers
- up to 20 km link distance

Voltage requirement (SIS3100)

+5 V < 2A single supply



Photograph of VME side

LEDs

10 front panel LEDs are implemented to visualise part of the SIS3100 board status.

LEDs of SIS3100	
A (VME slave access)	M (VME master)
P (power)	S (sequencer active)
R (ready)	L (link up)
LU (link sending)	LD (link receiving)
U (user)	DU (DSP user)

In addition 8 PCB SMD LEDs are implemented to visualise the link status in more detail

PCI Side

The PCI side of the SIS PCI to VME interface is named SIS1100 and consists of two printed circuit boards, which are available separately for other applications also. The first board is the SIS1100-CMC (common mezzanine card) carrier board, the second is the SIS1100-OPT Gigabit link CMC card.

- PLX9054 master PCI bridge chip
- PCI 2.1 and 2.2 compliant

LEDs of SIS1100	
A (VME slave access)	L (link up)
LU (link sending)	LD (link receiving)
U (user)	S (spare)

Software support:

- LINUX driver

Future option:

- NT driver

Interfacing options:

PCI-VME (SIS1100/SIS3100)

PCI-PCI (SIS1100/SIS1100)

PCI-Detector (SIS1100/SIS1100-OPT)

VME-VME (SIS3100/SIS3100)

VME-Detector (SIS3100/SIS1100-OPT)

Future interfacing options:

PCI-CAMAC (SIS1100/SIS5100)

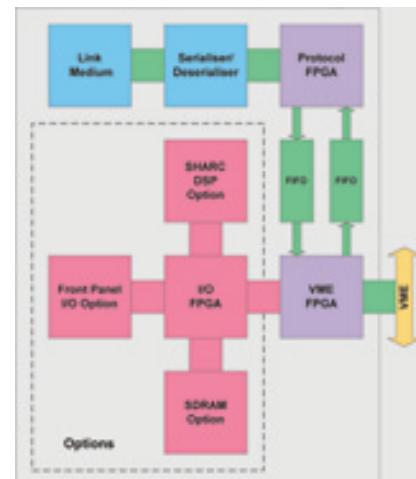
VME-CAMAC (SIS3100/SIS5100)

cPCI-VME (SIS1100-CPCI/SIS3100)

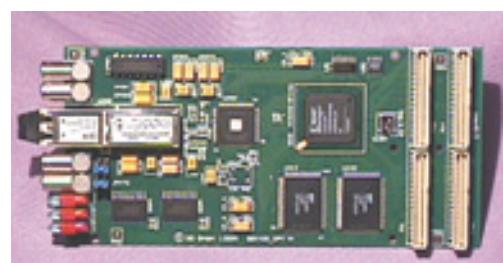
cPCI-Detector (SIS1100-CPCI/SIS1100-OPT)

cPCI-CAMAC (SIS1100-CPCI/SIS5100)

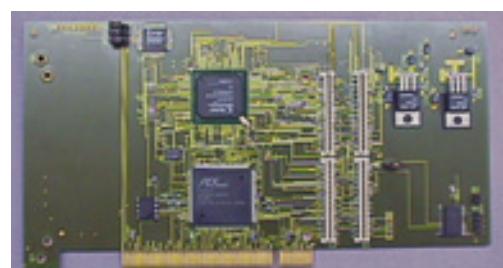
The SIS1100/3100 is a joined ZEL/FZ Jülich
SIS GmbH development



Simplified Block Diagram
of VME side (SIS3100)



Photograph of SIS1100-OPT



Photograph of SIS1100-CMC

100 MHz 12-bit VME ADC

SIS3300 Short Description

The SIS3300 is an 8 channel 6U VME digitizer/transient recorder with a sampling rate of up to 105 MHz and 12-bit resolution. The board has a width of one VME slot (4TE). The use of FPGAs for data handling and implementation of the VME interface allows for maximum flexibility.

Functionality

- 8 channels
- 12-bit resolution
- 1 to 105 MSamples/s per channel
- > 80 MHz analog bandwidth
- internal/external clock
- 128 KSamples/channel
- multi event mode
- event directory
- autostart capability
- pre/post trigger capability
- trigger output
- single width 6U VME card
- A32/D32/BLT32/MBLT64

Options

- LEMO00 connectors, 0 ... -5 V,
2.5 V ... -2.5V or 0 ... -1 V 50 Ohm inputs
- Differential LEMO connectors, input range
tbd.
- Dual memory bank (2 x 128 KSamples)
- stripped 4 channel version

Control In/Ouputs

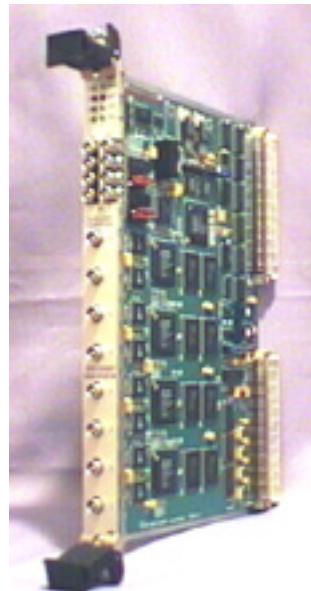
LEMO00 connectors are used for control input and output signals

Inputs:

- Clock In
- Start
- Stop
- User Input

Outputs:

- Clock out
- Busy
- Trigger
- User Output



Photograph of SIS3300

LEDs

8 LEDs are implemented to visualise part of the SIS3300 board status.

- A (slave access)
- P (power)
- R (ready)
- U (user)
- SAM (sampling)
- SRT (start)
- STP (stop)
- TRG (trigger)

Voltage requirement

+5 V single supply
6A @ 100 MHz