EXPERIENCE WITH THE NEW DIGITAL RF CONTROL SYSTEM AT THE CESR STORAGE RING*

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Abstract

A new digital control system has been developed, providing great flexibility, high computational power and low latency for a wide range of control and data acquisition applications. This system is now installed in the CESR storage ring and stabilizes the vector sum field of two of the superconducting CESR 500 MHz cavities and the output power from the driving klystron. The installed control system includes in-house developed digital and RF hardware, very fast feedback and feedforward control, a state machine for automatic start-up and trip recovery, cw and pulsed mode operation, fast quench detection, and cavity frequency control. Several months of continuous operation have proven high reliability of the system. The achieved field stability surpasses requirements.

INTRODUCTION

The Cornell Electron Storage Ring (CESR) is now operated in a multi-energy mode [1, 2]. This new operating regime puts new demands on the RF field control system; refer to [3, 4] for details. A new digital RF field control system has been developed at Cornell [3, 4], as a replacement of outdated analog control hardware. The new digital system provides the required flexibility with high computational power and low latency.

The digital control system was installed in the CESR storage ring in summer 2004, and since then stabilizes the vector sum field of two heavily beam loaded superconducting CESR 500 MHz cavities (loaded Q of $2 \cdot 10^5$ to $4 \cdot 10^5$; several 100 mA beam current).

We plan to use the new digital control hardware not only for the cavities in CESR, but also for the cavities in the Cornell ERL prototype [5] and ERL Light Source [6]. The cavity operation at a very high loaded Q_L in the ERL main linac is challenging and results in high demands for the RF control system. In a recent test we demonstrated that our system is capable to operate RF cavities at a loaded Q_L up to 10^8 with very good field stability [7]. In this paper we give an overview of the CESR RF control system, and discuss operational performance and experience from almost one year of operation.

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CORNELL'S DIGITAL RF CONTROL SYSTEM

Hardware

All digital and RF hardware has been designed in-house to maximize performance while keeping cost low. Figure 1 (left side) shows the schematic of the RF field control system for CESR. The right side of the same Figure shows a block diagram of the digital boards with their main components. The digital boards are discussed in detail in [3, 4].

All RF signals (klystron power signal, forward power signals, reflected power signals and cavity field signals) are down converted to an IF frequency of 12 MHz by high level mixers (Mini-Circuits ADE-10H) with good linearity. Special care has been taken to reduce noise contributions and to filer harmonics of 12 MHz. The IF signal preserves the amplitude and phase information of the original RF signal, and is sampled at a rate of 4*12 MHz. By this, subsequent data points describe the real (I) and imaginary (Q) part of the original RF signal. In addition to the seven RF signals, a klystron high voltage (HV) signal is sampled by a fast 48 MHz ADC (Analog-to-Digital Converter) after the signal has been passed through a high pass filter. This signal is used as input to a fast HV ripple compensation, as is discussed below. Further inputs to the digital boards are a trip input, cavity tuner positions and limit switches, cavity and coupler vacuum readings, klystron high voltage signal and timing signals. The digital boards have four fast DACs (Digital-to-Analog Converter): two to adjust the I and Q component of the vector-modulator (Analog Devices AD8345) output, and two DACs to regulate the drive voltage for piezo-elements in the frequency tuners of the two CESR cavities (for fast cavity frequency regulation). The output of the vector modulator drives the pre-amplifier for the klystron. The klystron output gets split equally to drive two CESR 500 MHz cavities in parallel.

Software

The control codes and logic resides in two FPGAs (Fixed-Point-Gate-Array) and two DSPs (Digital-Signal-Processor). The two FPGAs are performing the following tasks:

- decimation filters for all fast ADCs signals with signal calibration;
- proportional-integral (PI) feedback loop to stabilize the klystron output;

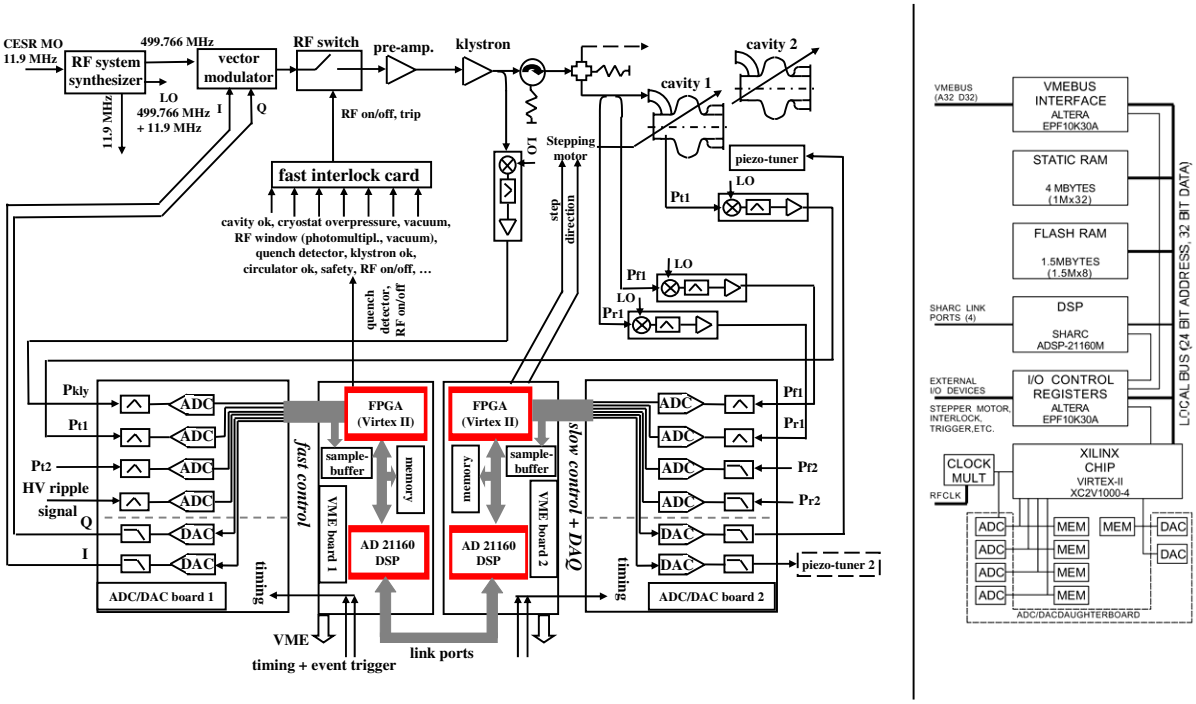

Figure 1: Left: Schematic of the digital RF control system for CESR-c. For simplicity the second RF cavity is indicated only. Right: Block diagram of the FPGA/DSP board.

- proportional-integral loop to stabilize the vector sum of the cavity fields;
- fast HV klystron ripple compensation to compensate perturbation from a significant ripple on the klystron high voltage.

The schematic of all feedforward and feedback control loops running in the FPGA is shown in Figure 2. It should be noted that the bandwidth of the klystron control loop and the cavity PI loop are quite different. The klystron loop is a high bandwidth loop (unity gain is at several 10 kHz), while the cavity loop has to run at much smaller gains with a bandwidth of less than one kHz. The reason for the small cavity loop bandwidth comes from the requirement that excitation of the beam at its synchrotron frequency has to be avoided. The beam is highly resonant at the synchrotron frequency of about 20 kHz. Smallest perturbations at that frequency will result in intolerable beam oscillation. For the cavity field this results in the requirement that the cavity field noise at the synchrotron frequency has to be below -220 dBc/Hz. Since realistic measurement noise will surpass this number, the way to achieve very low field fluctuation at the synchrotron frequency is to avoid any cavity feedback at this frequency at all by reducing the loop bandwidth.
The two DSPs are programmed in C, and are running higher level tasks, including:

- a state machine for automatic start-up and trip recovery;
- automatic loop phase calibration for the klystron loop;
- setting the klystron high voltage according to the required RF power (we operate the klystron with adjustable high voltage)
- adjusting an output rotation matrix to compensate for phase changes from changes in the klystron high voltage
- updating of the model used in the high voltage ripple compensation;
- trip and cavity quench detection;
- cavity frequency control (stepping motor driven and piezo-electric driven);
- pulsed cavity operation for cavity processing with pulse hight or width adjusted according to vacuum readings;
- data acquisition, down sampling, and peak detection;
- ring buffers of all sampled data (100 kHz sample rate, 1 second deep).

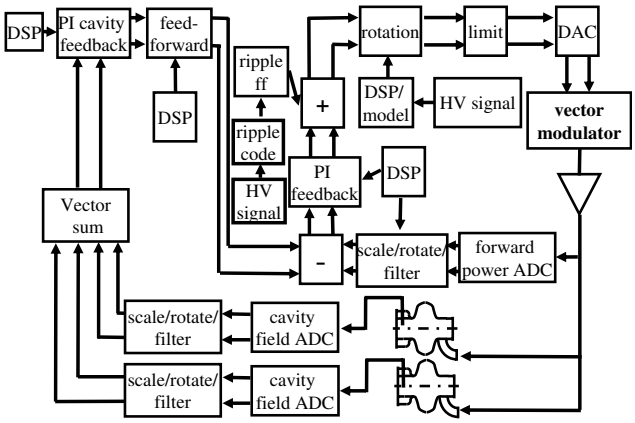

Figure 2: Schematic of the feedback and feedforward control loops.

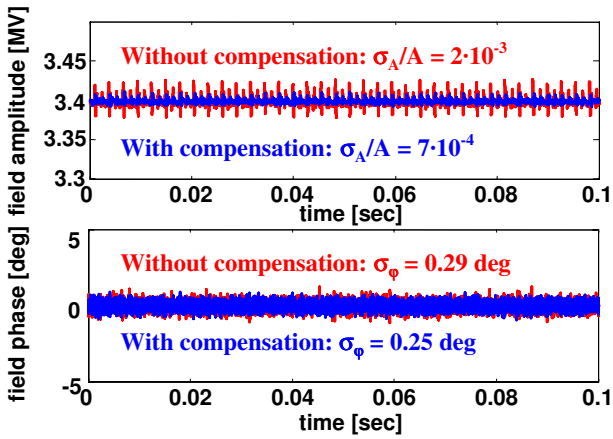

Figure 3: Measured amplitude and phase stability without and with HV ripple feedforward compensation.

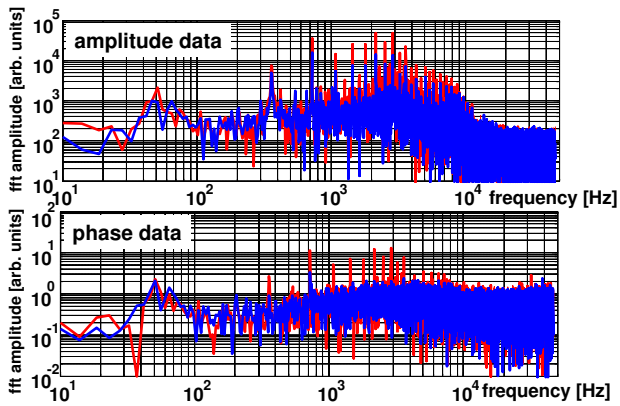

Figure 4: Fourier spectrum of the time domain signals shown in Figure 3.

CESR RESULTS

The new digital RF field control system has been installed in Summer 2004 in the CESR storage ring, and is in operation since then. After some initial problems (software related and a faulty power supply), the system is running very reliable. No unplanned down time has been caused by the digital system in the last six months.

From start on the system surpassed the required field stability of 1% rms in relative amplitude stability and 0.5° rms in phase stability, see Figure 3. It should be recalled that this was achived with fairly low gains to achive unity gain below 1 kHz to avouid excitation of synchrotron beam oscillations. While the phase noise is dominted by noise on the CESR reference system, the major contributor to amplitude fluctuations was found to be caused by a fast ripple on the klystron high voltage. The HV ripple causes fluctuation of the klystron output, which then modulates the cavity field. This modulation has frequency lines in the kHz range, as can be seen from Figure 4. To further suppress this field fluctuation we added a feedforward compensation. The feedforward algorithm uses the measured high voltage fluctuation as input and applies feedforward to the klystron loop, see Figure 2. A simple mathematical model for the klystron is used in the feedforward algorithm. The improved field stability with applied HV ripple feedforward is obvious from Figure 3.

OUTLOOK

The digital CESR RF field control system is in operation, and has proven high performance and good reliability. In the future we plan to further explore its performance. This will include testing more complex control algorithms for the klystron and cavity feedback loops, an improved RF reference system and studying active microphonics compensation.

REFERENCES

[1] D. Rice, Proceedings of the 8th European Particle Accelerator Conference 2002, Paris, France, p. 428 (2002).

[2] S. Belomestnykh, Report SRF020918-06, Cornell Laboratory for Elementary-Particle Physics (2002).

[3] M. Liepe et al., Proceedings of the 2003 Particle Accelerator Conference, Portland, Or, USA (2003).

[4] M. Liepe et al., Proceedings of the 11th Workshop on RF-Superconductivity, Travemuende, Germany (2003).

[5] G. Hoffstaetter et al., Proceedings of the 2003 Particle Accelerator Conference, Portland, Or, USA (2003).

[6] G. Hoffstaetter et al., this conference, paper RPPT026.

[7] M. Liepe et al., this conference, paper WPAT040.