FACILITY WIDE REAL-TIME BEAM LOSS MONITORING & CONTROL USING FPGA TECHNOLOGY

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Abstract

The ISIS facility based at Rutherford Appleton Laboratory, Chilton, Didcot, UK is currently the worlds brightest pulsed neutron spallation source producing a beam to target power of ~160kW. Whilst operating at high beam powers it is critical that beam loss around the facility is monitored to ensure that component activation is kept to reasonable levels. Beam loss is detected using 82 gas ionisation chambers distributed throughout the Injector, 800MeV Synchrotron, the Extracted Proton Beamline and the new Extracted Proton Beamline for the second target station (TS2).

This paper introduces the new Beam Loss Display and Beam Trip systems which use a modern Field Programmable Gate Array (FPGA) design to provide real time monitoring, beam loss data logging and faster beam trip reaction time. Bench testing has proven the new system.

INTRODUCTION

Background Motivation

ISIS is currently the world brightest neutron spallation source producing a mean power of ~160kW. ISIS consists of a 665keV Radio Frequency Quadrupole (RFQ) feeding a 70MeV LINAC injected into a rapid cycling 50Hz Synchrotron; producing 800MeV protons at 200 μA to a tantalum target.

ISIS is currently undergoing a number of significant modifications; the addition of second harmonic accelerating cavities in the Synchrotron will increase the potential beam current to 300μA. In addition a large scale building project, to be completed at the latter end of 2007, will provide a second target station optimised for long wavelength neutron experiments.

As machine power increases it is important to ensure that beam losses are tightly monitored and controlled, guaranteeing that ISIS does not suffer component damage and/or high levels of component activation, both of which would be detrimental to the operation of ISIS as a hand on maintained machine.

Diagnostic Upgrade

The new design is an extension of a prototype designed to display four beam loss plots for the Synchrotron [3]. The new design uses the same video processing architecture as the prototype and includes the ability to trip the machine, communicate trip information to a local National Instruments PXI computer and display a single real time plot of beam loss data.

BEAM LOSS MONITORING

Detectors

Beam loss is monitored using a total of 82 beam loss monitors (BLM) located in four areas of ISIS.

- Injector - 17 BLMs
- Synchrotron - 40 BLMs
- EPB1 - 10 BLMs
- EPB2 - 15 BLMs

The types of monitors used are 3-4 metre long argon filled ionisation chambers of the Brookhaven design [1]. The BLM detects evaporation neutrons from the point where a proton has interacted with a part of the machine [2] as the neutron passes through the argon an interaction occurs with the nuclei of the gas [1] producing a current in the range 1nA to 1μA.

Signal Conditioning

There are two systems employed to provide BLM data to diagnostic equipment. Firstly a close coupled, low noise head amplifier [1] converts the low current BLM output into a differential voltage in the range 0 – 10V. The voltage signal is provided to a sample and hold buffer where it is integrated over a variable period and sampled. The sample pulse is provided by ISIS timing modules allowing the integration period and sample point to be varied with reference to the machine cycle.

BLM Displays

The current display system in the MCR uses three fast vector scan Visual Display Units (VDU) to display BLM data for the Injector, Synchrotron and EPB1. Each VDU displays BLM data and tolerance level settings on a monochromatic screen at a refresh rate of half the machine frequency (25Hz). Figure 1 shows an existing display in operation at the MCR.

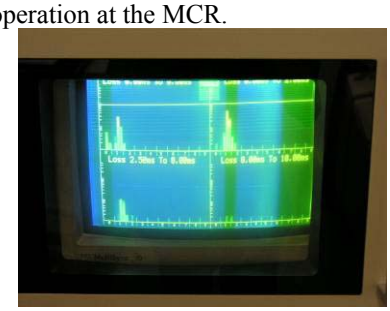

Figure 1: Existing BLM Display.

Diagnostic Machine Protection

Beam warnings and beam trips are driven by comparing BLM data to individual tolerance levels. The comparison is executed at the machine frequency; a warning is produced when a tolerance level is initially exceeded, a trip signal is asserted when a tolerance level is exceeded over a consecutive number of machine cycles. The trip signal must be generated within 10ms of a trip event occurring. Both warnings and trips are only asserted once within a machine cycle.

BEAM LOSS MONITOR & BEAM TRIP UPGRADE

Overview

The existing BLM system was designed for ISIS as a single target facility; the inclusion of a second target requires a fourth system to provide BLM data for EPB2. Investigation of the current system highlighted that the processing hardware was obsolete, this coupled with a dated display unit made the system ideal for upgrading.

The design for the new system was required to replace the three existing BLM displays, diagnostic protection hardware and provide a fourth system for EPB2. In doing so the new system should follow the functionality of the previous system and provide additional features, in particular:

- Produce data on a modern display
- Display Real Time Data
- Integrate diagnostic protection and display hardware
- Provide a trip signal within 10ms
- Visually indicate a tolerance excursion
- Freeze display after trip event
- Transmit over tolerance channel after trip event

Figure 2 highlights the BLM display and trip system. It should be noted that there are four identical systems located around the facility each driving a separate BLM display located in the MCR. The BLM head amps, signal conditioning units, Beam Permit System (BPS) and PXI units are all local to the BLM display and trip systems.

System Hardware Overview

The FPGA design is split into a number of core components; BLM display generation, BLM trip generation, acquisition of BLM data (DAQ) and serial communications.

The display and trip components utilise the majority of the FPGA design. Both components share the read data and address busses for two Dual Ported Read Access Memories (DPRAM) storing BLM data and BLM tolerances. The address bus is controlled by either the display or the trip components with the trip design having the highest priority access. Access is asynchronous with respect to each component; therefore the trip system will take control of the address bus whilst the display component is writing to the monitor. Due to high speed comparators used in the trip design the period that the display design looses control of the bus is ~1μs; this is not noticeable to the human eye.

Data Acquisition & ADC Control

BLM data is acquired via a bank of five, 12 bit, eight channel serial Analogue to Digital Converters (ADC). ADC control lines are shared by all ADC allowing eight channels to be acquired in parallel.

The FPGA design generates the control signals to the ADC, decodes serial data and writes to the subsequent areas of BLM DPRAM. These processes are initiated after a sample pulse is provided to the BLM system. Due to the programmable nature of FPGA this scheme allows a number of options to be implemented for data acquisition. Testing highlighted that good results were

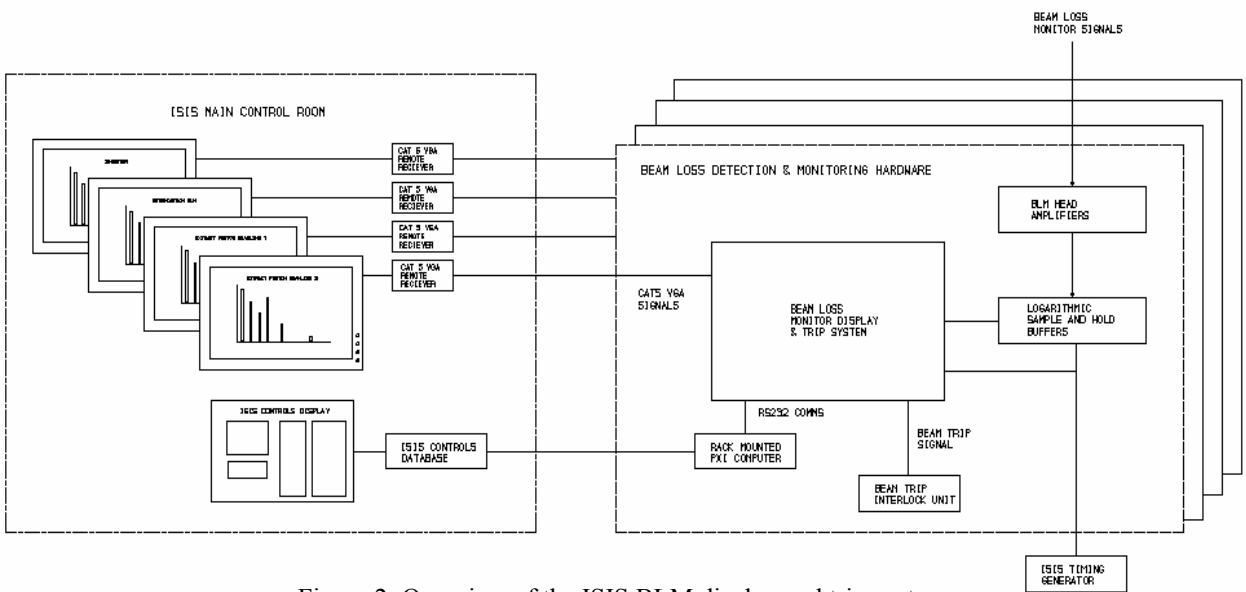

Figure 2: Overview of the ISIS BLM display and trip system.

gained from a sample clock frequency of f_S=12.5MHz, providing acquisition of all BLM channels in t_{DAQ}=13µs.

Video Processing & Display

Four 15" TFT monitors will be installed in the MCR to replace the old VDUs, the displays are located up to 200 metres from the driving source; therefore CAT5 VGA splitters have been used to extend the distance video signals can be transmitted.

The FPGA design is responsible for interpreting data and producing a Video Graphics Array (VGA) standard video signal, the design implements a field resolution of 640x480 pixels with the potential to display 24bpp (bits per pixel) Truecolor.

The display generated by the FPGA is shown in figure 3, BLM voltage is presented as a histogram on a $\log_{10}$ scale. BLM tolerances are displayed as a blue dash for each histogram bar, healthy beam loss is indicated by a green colour, unhealthy beam loss is related to an excursion through a tolerance and is represented by a red colour. Unhealthy beam loss indicates that a trip event is on the horizon. If a trip event does occur the display will freeze indicating the last BLM that detected unacceptable beam losses.

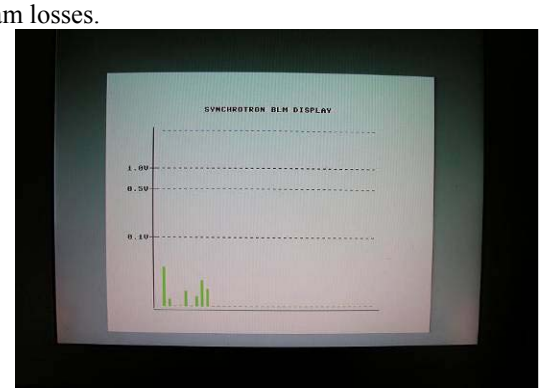

Figure 3: New BLM Display.

Beam Warnings & Trip

There are two types of beam warnings; fast and slow. The fast warning system is handled by the BLM system indicating which BLM channel caused a trip by transmitting a flag and BLM channel number to the ISIS control system via a local PXI. The slow warning system is handled by the PXI which records average beam loss over 30 seconds, 4 minutes and 20 minutes; producing a trip signal if average loss exceeds the average tolerance level.

Beam trips are generated by the FPGA design when BLM data exceeds its tolerance level over a number of consecutive machine cycles, both tolerances and excursion limits are programmable via serial communications to a PXI. When a trip event has occurred the FPGA produces a double pulse TTL signal to the BPS to indicate that the machine should be tripped. Only one trip per system per machine cycle can be generated. Due to the high speed video clock that was utilised for the trip hardware the new system is able to produce a beam trip signal within ~14µs of a trip event being detected.

ISIS Controls Interface

ISIS has an extensive control network providing access to a large number of diagnostic and control equipment via a touch screen interrogated database located in the MCR. It is necessary to provide a link between the controls network and the BLM display and trip systems allowing tolerance and excursion limits to be set, and trip/warning information to be processed. The link is provided by a PXI system which extracts values from the database and constructs serial packets to be decoded by the FPGA Universal Asynchronous Receiver/Transmitter (UART) and vice versa. Data from the BLM system is sent within 1 second to meet with the update frequency of the controls database.

CONCLUSION

Beam loss monitoring and its associated machine protection electronics is an extremely important part of ensuring activation levels are kept to reasonable levels, enabling ISIS to remain 'hands-on' throughout increasing beam currents. The upgrade of the BLM display and trip systems provides real time monitoring with a faster beam trip reaction time. The nature of FPGA technology provides in system programmability giving scope to meet future requirements if necessary.

ACKNOWLEDGEMENTS

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REFERENCES

[1] M.A. Clarke-Gayther, A.I. Borden and G.M. Allen, "Global Beam Loss Monitoring Using Long Ionisation Chambers at ISIS.", EPAC'94, London, July 1994, p. 1634.

[2] C.M. Warsop, "Studies of Beam Loss Control on the ISIS Synchrotron.", EPAC'04, Lucerne, July 2004, p. 1464.

[3] M. North, A. Kershaw, "Real-Time Beam Loss Monitor Display using FPGA Technology", PAC'05, Knoxville, May 2005, p. 2914.

