ALS MINI IOC: AN FPGA EMBEDDED PROCESSOR BASED CONTROL SYSTEM MODULE FOR BOOSTER MAGNET RAMPING AT THE ALS*

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Abstract

The Advanced Light Source (ALS) booster magnet upgrade for top-off operation [1] requires new instrumentation to meet increased magnet ramping requirements. To address these requirements, the ALS Instrumentation group and Control Systems group collaborated to design a new control system module called the Mini IOC. The Mini IOC hardware is based on a commercial evaluation board containing an FPGA with embedded processor and built-in interfaces for 64MB of DDR SDRAM and Ethernet. A custom module is used for analog controls and monitors. The PowerPC® embedded processor runs an EPICS [2] database built on the VxWorks operating system allowing remote access via Ethernet. This paper includes an overview of the Mini IOC design and operational results.

INTRODUCTION

The ALS at Lawrence Berkeley National Lab (LBNL) has been operating since 1993 providing synchrotron light to experimenters. Operationally, a booster synchrotron is used to fill a storage ring every 8 hours. During one of these fill cycles, individual magnet power supplies follow the main bend magnet as it ramps to maximum current.

A project for continuously filling the storage ring called top-off is currently underway at the ALS. For top-off, booster magnet power supplies will each be controlled independently with their own ramp profile, rather than following the bend. A master trigger synchronizes the start of all ramps and very accurate local clocks in each controller ensure adequate ramp tracking across power supplies.

The large power supplies (the main bend and two quadrupole supplies) were replaced to meet the top-off requirements. The remaining 40 smaller supplies for corrector magnets were not replaced, but their controllers have been upgraded to accommodate the new ramping scheme. To avoid replacing the existing power supply controller infrastructure, the new controller is designed to be plug-compatible with the original controller. In addition to handling the required ramp generation, the new controller runs an EPICS control system interface, which is compatible with ALS control system requirements. This new power supply controller is called the ALS Mini IOC.

DESIGN REQUIREMENTS

The ALS control system actually consists of two separate systems: the original system, based on the in-house designed Intelligent Local Controller (ILC) [3], and a conventional EPICS system with bus-based I/O Controllers (IOCs), such as VME or CompactPCI (cPCI), running the real-time operating system VxWorks. The ALS Control Systems group requires that new and upgraded hardware connect to the EPICS system.

For top-off, the booster corrector magnet ramp profile consists of a 10,000 point table of current steps, each step occurring at a fixed time interval starting with a common start pulse. Each controller is responsible for controlling up to four power supplies. The corrector magnet power supplies were originally controlled by 20 ILCs, but they were not equipped to support the top-off requirements. Additionally, it was desirable to upgrade the controllers to be compatible with the EPICS integration requirement.

The original cost estimate for replacing these ILCs was based on deploying 4 of our standard cPCI bus-based IOCs, which included significant cost to re-wire the system. We determined that by using Field Programmable Gate Array (FPGA) embedded processor technology, we could build a new controller, the Mini IOC, to be plug-compatible with the ILC and have the capability to run EPICS for about the same cost as the standard cPCI solution.

HARDWARE

An FPGA with embedded processor was selected as the foundation of the Mini IOC since it is able to handle the booster ramp requirements and the control system interface in a single chip. A large DRAM was required to store control system software and a small flash memory for boot software. We also needed four channels of 16-bit 10kHz analog output per module to ramp four magnet power supplies, and some digital I/O for additional control and monitoring. Analog input was desirable for current monitoring.

The Mini IOC hardware block diagram is shown in Figure 1. For the digital and control system components of the design, we selected the Avnet Mini-Module, a commercial module with a Xilinx® Virtex™-4 V4FX12-SF363 FPGA with embedded PowerPC® PPC-405, Platform flash for FPGA configuration, 64MB DDR SDRAM, 4 MB flash, and Ethernet PHY and connector, all in a very small form factor [4]. For the analog portion of the design, we elected to use two previously built in-house designed IndustryPack (IP) Modules per Mini IOC. Each IP Module contains two 16-bit 100kHz DAC channels and one 16-bit 40 kHz four channel ADC.

We then designed a new custom motherboard with sockets for the Avnet Mini-Module and dual IP Modules. To this we added two port expanders for digital I/O, a system monitor for ambient temperature and supply voltage monitoring, an RS-232 console port, a JTAG port

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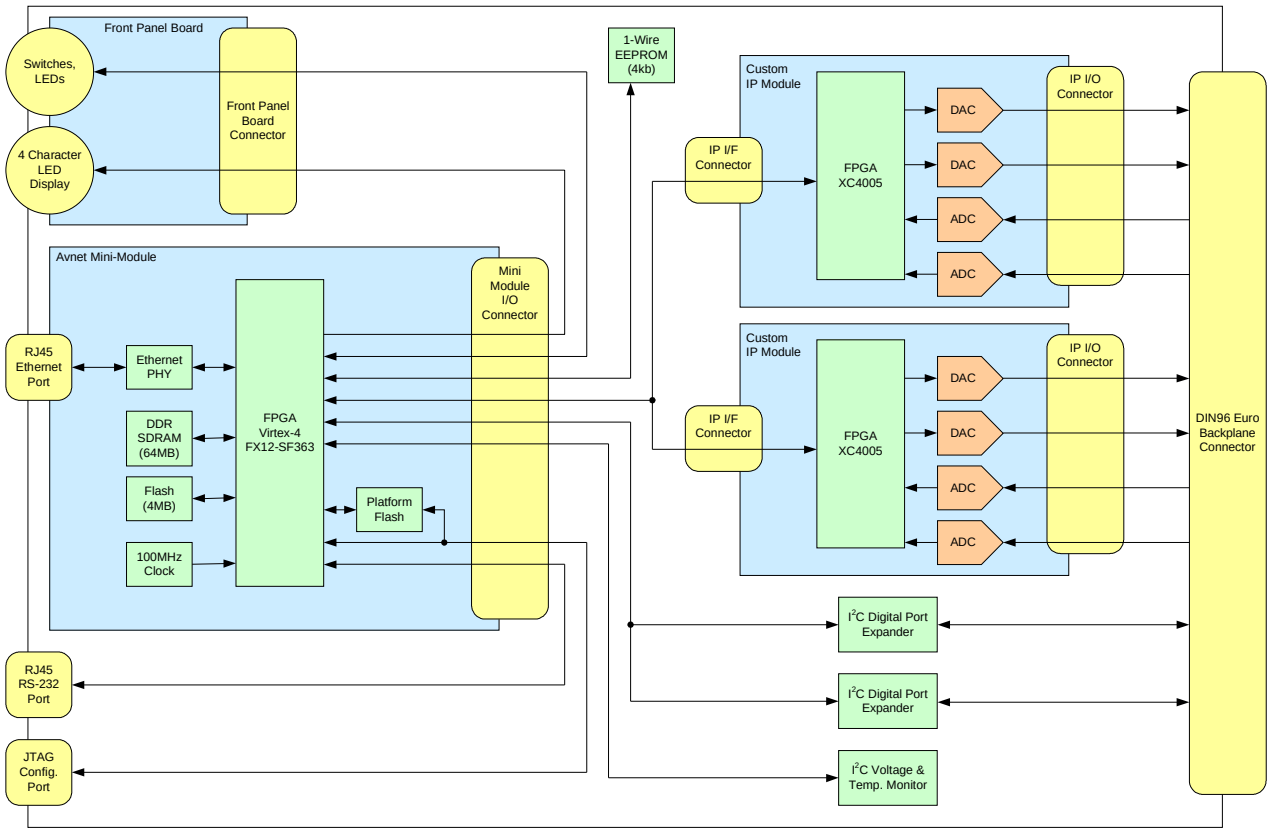

Figure 1: ALS Mini IOC Hardware Block Diagram. The Mini IOC Base Board (outer rectangle) contains connectors for the Avnet Mini-Module, two IndustryPack (IP) Modules and a front panel module.

for FPGA configuration, and a front panel module with status LEDS, a 4 character LED display, and reset and general purpose switches.

LOGIC DESIGN

A typical FPGA embedded processor design consists of a processor connected via internal buses to peripherals (cores) that control various hardware interfaces. The Mini IOC FPGA firmware block diagram is shown in Figure 2 and the embedded design and development is discussed further in [5]. In the key, a "Xilinx core" refers to a core designed and supplied by Xilinx® with customized parameters for this design. These cores include the embedded PowerPC® processor, Ethernet MAC, RS-232 UART, memory controllers (DDR SDRAM, flash, block RAM), as well as the bus structures and bus bridge. A "custom core" indicates a core built from a bus interface template supplied by Xilinx® that contains logic primarily designed at LBNL. These interfaces include the Booster Ramp, I^2C (system monitor, digital I/O), 1-Wire EEPROM, IP Module, and LED Display controllers.

Most of the custom cores are bus slaves—responding to transaction requests received over the bus, but not initiating any transactions—which are easier to implement. The exception was the Booster Ramp controller core, which was more complex to implement both because it is a bus master and a complex functional block.

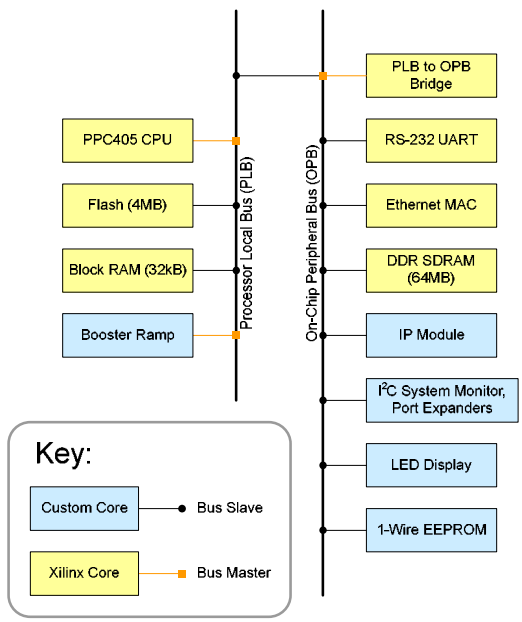

Figure 2: ALS Mini IOC FPGA firmware block diagram.

Booster Ramp Controller

The Booster Ramp controller core needed to be a bus master to transfer ramp table data from the DDR SDRAM and to the DACs via the IP Module interface. Figure 3 shows the state machine that controls the timing of data transfers in the core. The state machine waits for the booster waveform trigger from the ALS Timing System to

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initiate the ramp cycle. Next, the bus master transfers the first data point for each of the four ramp channels from DDR SDRAM to registers in the Booster Ramp core. The state machine then waits for the output point time interval trigger. Once received, the bus master transfers the scaled data to the IP Module interface to be sent to the DACs. The points are sent out at each output point time interval until the ramp cycle is complete. At this time the state machine is reset to the initialized state and awaits the next booster waveform trigger.

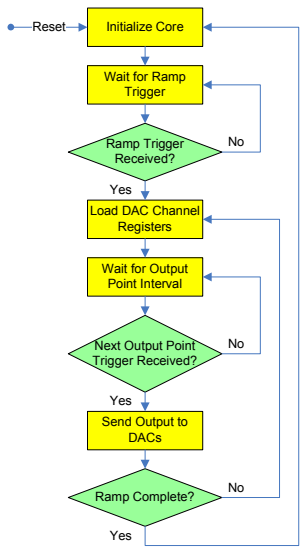

Figure 3: Booster Ramp Controller simplified state machine.

The data path of the ramp table data in the Booster Ramp controller is shown in Figure 4. A 16-bit value representing one point of each of four channels is transferred sequentially from the DDR SDRAM via the Processor Local Bus (PLB) to separate registers in the Booster Ramp controller. When the ramp point time interval is reached, each value is sequentially scaled by the corresponding channel gain factor and sent back over the PLB to the IP Module and ultimately written to the corresponding DAC. This process must be sequential because all four DAC channels share a single IP bus and only one DAC can be written per IP bus transaction cycle.

OPERATIONAL EXPERIENCE

The installation of the Mini IOCs has been largely successful, after some initial software problems. After putting the Mini IOCs into production at the ALS in January, 2007, we began to experience sporadic software failures where the VxWorks network servicing task (tNetTask) would suspend operation on an ENOBUFS error after several hours to several days of operation. While the Booster Ramp controller and other logic continued to function without interruption, network control via EPICS would be lost until the IOC was rebooted. Various debugging attempts were made, but none had any effect until the XEM_MIN_RECV_BUFS and XEM_DFT_RECV_BUFS values were increased (to 64 and 128, respectively) to add DMA receive buffers in the xemac (Ethernet) driver. Since that change was made in early March, we have not experienced a repeat of this problem. We also deployed a Mini IOC to control the upgraded booster RF system [6] because the ramping requirements of the booster RF and the corrector magnets are similar.

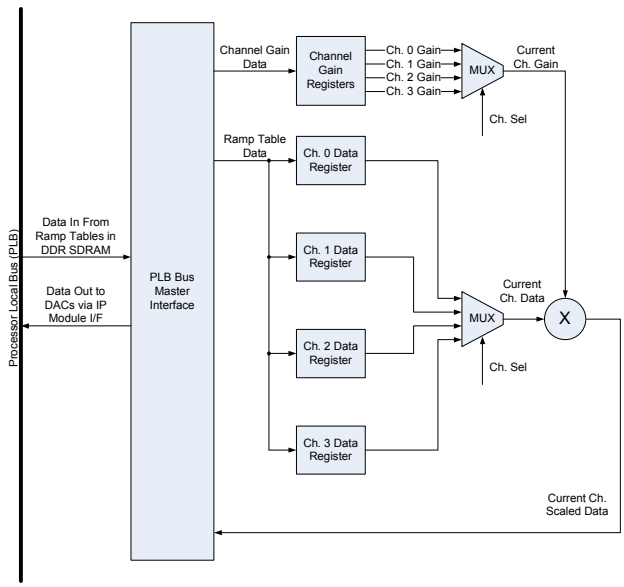

Figure 4: Booster Ramp controller data flow.

CONCLUSION

The Mini IOC project was successful on several fronts. Using a commercial FPGA module minimized board design risk resulting in a working design on the first board fabrication. Since the initial software problem was resolved, the controllers have been operating consistently and to specification. Success with this design gives the ALS confidence to consider using FPGA embedded processor technology for future control system instrumentation designs.

REFERENCES

[1] D. Robin, et al, “Plan to Upgrade the Advanced Light Source to Top-Off Injection Operation,” EPAC’04, Lucerne, Switzerland, 2004.
[2] L. R. Dalesio, et al, “The Experimental Physics and Industrial Control System Architecture,” ICALEPCS’93, Berlin, Germany, 1993.
[3] S. Magyary, et al., “Advanced Light Source Control System”, PAC’89, Chicago, IL, 1989.
[4] Avnet Product Brief: Xilinx® Virtex™-4 Mini-Module, http://www.em.avnet.com.
[5] J. Weber, et al, “Hardware and Software Development and Integration in an FPGA Embedded Processor Based Control System Module for the ALS,” these proceedings.
[6] K. Baptiste, et al, “Results of the ALS Booster Ring RF System Upgrade for Top-Off Mode of Operation,” these proceedings.

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