DEVELOPMENTS IN HIGH-PRECISION ASPECTS OF POWER CONVERTER CONTROL FOR LHC

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Abstract

The initial results from integration testing of the LHC magnet power converters revealed problems of low-frequency noise, settling time, drift with time and temperature, thermal management and EMC. These problems originated in the use of DSP, the A/D converter (ADC), the DCCT and their respective environments. This paper reports the methods used to improve the performance through hardware and software modifications and the results achieved.

INTRODUCTION

Already at the design stage it was known that the LHC power converters required a different approach from earlier accelerators due to the underground installation, the superconducting loads, the higher accuracy requirements and the large number of circuits. Earlier reports [1] have described the design approach and the reasons for the choices made. Some of the key choices were: very compact, light and high efficiency design of the power part requiring switch-mode technology, load time-constants up to many hours and accuracy of a few ppm (10^{-6}) with excellent tracking between power converters requiring digital current control loops, two redundant current transducers (DCCT) for accuracy verification. Consequences that could be expected from a compact underground installation were thermal management problems, short-term drifts and electromagnetic compatibility problems. Efforts were made at the design stage to cover these types of problems, but the reality could only be analysed properly once integration tests of the different subsystems started at CERN. To optimise the precision requirement four accuracy classes were created, corresponding to the converter types: 13kA, 4-7kA, 600A and 60/120A. The half-hour overall stability target was respectively 3, 5, 10 and 50ppm.

NOISE, DSP AND ALGORITHMS

The ADCs and the DCCTs were evaluated at an early stage and their calibration as well as output noise spectra were established, but in a benign laboratory environment. When they were deployed together for the first time and the digital control loops closed, the converter output LF noise was many times higher than expected and the DC values could be off by tens of ppms. Long campaigns were necessary to identify the several causes and make improvements. Below follow some detailed cases.

The 13 kA converter calibration was off target by 10-30 ppm. The cause was a common mode emission from the input of the 22-bit Delta-Sigma ADC (1 MHz clock) causing rectification in the input stage of the output amplifier of the measured DCCT. The input of the ADC was equipped with an EMC filter and the output of the DCCT likewise. The shielding connections were also tested with a burst generator and then optimised. The errors could then be made smaller than 0.1 ppm.

DCCTs were disturbed by high-frequency common mode currents from the switch-mode power part passing through the head, giving offsets of more than 10 ppm. The power part output filter was improved/reconfigured, the shielding of the DCCT head and cable was improved and the ground connections were optimised.

The initial high noise seen was due to EMI (burst type) and current loop setup (constant high noise). The first problem was solved by increased shielding of all the reference instrumentation and then a loop optimisation was done for each converter type, leading to an overall noise figure slightly bigger than the ADC alone.

The 22-bit ADC showed a resolution loss at 10V. The digital output was formatted as an 8 character string, including the decimal point, so its resolution was 0.1ppm up to 9.999999V and 1ppm above 10.00000V. A simple software change fixed the problem.

The noise the 16-bit SAR ADC was ±3 bits, but thanks to the SAR's high speed, it could be lowered by averaging n samples. As CPLDs can not be used in radiation hard designs, this task had to be carried by the DSP. The number of samples in the average was thus limited by the available processing time to 3, giving a noise reduction of 40%.

Both static and tracking errors were observed inside the digital current loop [2]. They were unexpected, as the loop had been simulated and analysed completely in a PC based environment. The loop was set up as a PII (double integrator), thus ensuring the absence of both errors, but its 32-bit floating point implementation led to arithmetic errors, which could not be eliminated by rearranging operations, nor rescaling signals, without worsening the loop behaviour. A deep analysis, using a custom JAVA simulator that was capable of dynamically selecting the resolution and the storage size of variables, showed that the way the integrators were implemented was responsible for the errors. The resolution-related loss of signal acted as a parasitic path that limited the controller gain, upsetting the desired double integrator performance. Hence, the implementation of the integrator was changed, using an explicit integration formula, calculating and storing the accumulated value in 64-bit floating point. Further, a PIII (triple integrator) loop was implemented [3], aiming at zero dynamic error during a parabolic ramp,

which is important for LHC. Both static and dynamic errors were removed, as proved with warm magnets and a generally better noise performance was achieved. Level-dependent noise that had been observed on some converters was also cured by this implementation. These improvements were confirmed with superconducting loads during the hardware commissioning phase. The next step will be to merge the two loops into a single one, giving the elegance of the RST [2] approach and the better arithmetic behaviour of the PIII.

PERFORMANCE MONITORING TOOLS

It was essential to monitor the FGC measurements and regulation algorithm, so a test connector with a serial link directly from the DSP was included. This continuously provides six 32-bit floating point values at 1kHz. The user can choose any signal from a list of more than 30 on any channel.

To acquire these signals the user needs a PC and an FGC USB interface. This plugs onto the FGC front panel and appears as a virtual COM port under Windows or Linux. A graphic interface has been written under Labview (FGCspy), fig. 1, that can acquire up to 1M samples at 1kHz. The USB interface can also be instructed to sub-sample the data if really long acquisitions are required.

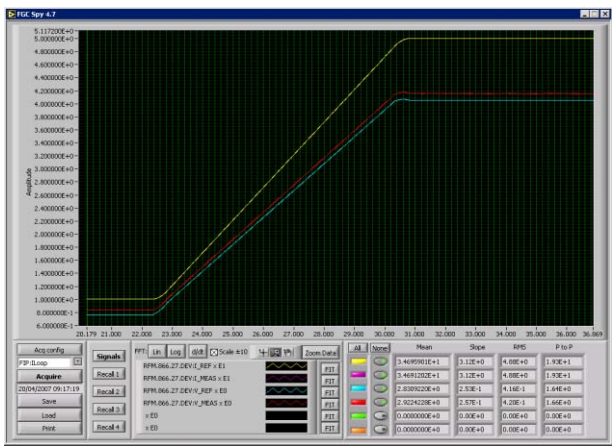

Figure 1: FGC Spy Interface

FGC Spy Interface

Once the Spy interface has acquired a period of data it can do all the usual manipulations: zoom, auto-scaling, FFT with log or linear frequency axis, derivatives, first order fit, noise analysis (p-p and RMS) and data export.

Since the FGC acquires data at 1kHz and its analogue inputs have only first order anti-aliasing filters, care must be taken when interpreting noise peaks.

Remote diagnostics

The vast majority of the ~1700 FGCs installed in the LHC are underground and difficult to access. Every FGC is connected to the controls network via a WorldFIP 2.5Mbps Fieldbus. Between the Ethernet and each WorldFIP segment there is a gateway computer, and every segment can support up to 30 FGCs spread out over up to one kilometre.

Every FGC includes 448kB of memory for signal logging. This is dedicated to circular buffers that record all the important signals acquired or calculated by the FGC. The main purpose of these buffers is to provide log data for the LHC post mortem system in the event that the converter trips or the beam is lost. However, it is also possible to read these logs on demand without stopping the logging. The readout rate is limited by the FGC's share of the bandwidth of the WorldFIP Fieldbus (6kB/s).

SETTLING TIME AND TEMPERATURE DRIFTS

FGC problems

Analog high-precision circuits require a well defined ambient. In a large power converter there is normally no problem to reserve a corner with good ventilation where the electronics can be located. The electronics will then only see the ambient temperature variations. In the compact designs required for the LHC installation it is no longer possible to have this separation and the variable internal power dissipation will create much larger temperature variations.

First tests showed a clear temperature dependency problem and 11 random FGCs were chosen for tests in a thermo-regulated oven. The FGC chassis was equipped with speed-controlled fans to minimise the impact on the voltage references' temperature control. Each FGC was also fitted with a small deflector to avoid blowing air directly on the components.

The FGC internal voltage references and the ADCs' output were then measured w.r.t. temperature variations in the oven, see table 1. TC is the linear temperature coefficient (ppm/K) and ΔTC the curvature (ppm).

Table 1: TC and ΔTC measured on 11 FGCs

	TC_A	ΔTC_A	TC_B	ΔTC_B
Mean	-2.0	1.4	-2.0	1.4
Std Dev	0.3	0.4	0.2	0.4
unit	ppm/K	ppm	ppm/K	ppm

The main conclusions were as follows. The operating range of the voltage references' temperature control is 19…37ºC. The ADC's offset TC is < ±0.5ppm/K and the TC of the reference voltages is < ±1ppm/K, so both are ignored. The ADC's gain TC is temperature dependent, but a second order model fits quite well. The TC value is from between -1.5 and -2.5 ppm/K @ 19°C to -3.5 to -4.5 ppm/K @ 37°C.

These results showed the importance of the fan tray as well as the air deflector in achieving reasonable working limits for the temperature control. They also showed that a compensation for the ADC gain error was necessary.

TC compensation algorithm

The FGC includes an inlet air temperature sensor (DS18B20) connected to a Dallas 1-wire bus. This provides a measurement of the temperature every 10s with a resolution of 0.0625°C and an absolute accuracy of ±0.5°C. Using this measurement, it is possible to compensate for part of the error due to the TC of the analogue measurement components [5].

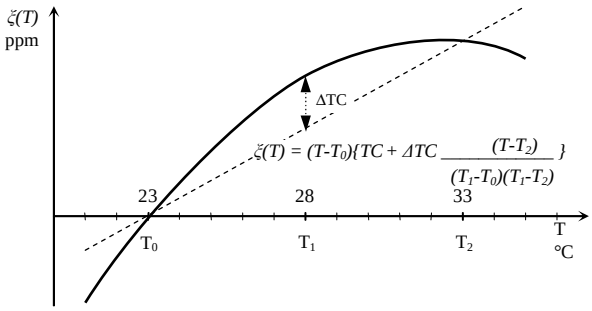

Figure 2: Second order temperature compensation model

A second order model was chosen for the error as a function of temperature. This is shown in Fig. 2 and is based on three fixed temperatures, T_0, T_1, and T_2 which were chosen to be 23, 28 and 33°C. The temperature error $\xi(T)$ is zero by definition at T_0 and the second order component is zero at T_0 and T_2. The degree of non-linearity is defined by an offset, ΔTC, from a straight line at T_1, This model can be applied to the offset, positive gain and negative gain for the ADC as well as the DCCT.

TC algorithm evaluation

After the introduction of the compensation algorithm, a test campaign was carried out to verify its implementation in the FGC. During the first test campaign the values of the TC and ΔTC for each FGC were measured. For an accurate verification of the algorithm, these individual TCs and ΔTCs were used, rather then using the average values given in table 1. Four FGCs were then evaluated with and without the correction using the same test setup as in the previous test.

The results showed that the algorithm was successfully implemented, but also stressed the difficulty in precisely determining the TC and ΔTC, as pictured by the residual errors showed in table 2. The table shows the maximum error in the range 23…33ºC with the ADC gain calibrated at 23ºC.

Table 2: Max errors in ppm before and after correction

	ADCA before	ADCA after	ADCB before	ADCB after
FGC 1	-19	-4,1	-24,6	-4
FGC 2	-25,9	-3,4	-22,2	-2,8
FGC 3	-20,5	0.8	-20,4	0
FGC 4	-23,1	-2,5	-19,4	-2,1

The use of individual TCs for the correction means that a good method to measure the TC and ΔTC of a thousand FGCs would have to be found. A first attempt to do this by varying the ambient temperature in an entire equipment gallery failed. For this reason, it was decided to use the average values listed in table 1 for all units as well as channels A and B.

Fig. 3 shows the result of applying a standard correction to an FGC with the data below:

TC_A = -1.5ppm/K and ΔTC_A = 1.5ppm

TC_B = -2.0ppm/K and ΔTC_B = 1.7ppm

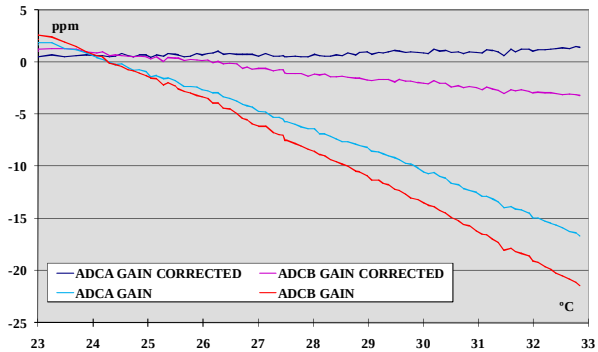

Figure 3: FGC gain error with and w/o correction

CONCLUSIONS

- DSP applied to high-precision regulation introduces a new set of problems. The learning period is measured in years.
- Floating point arithmetic can lead to unexpected behaviour. Results may not be the same as PC-based simulations.
- On-line diagnostics tools should always be included in a DSP design
- The problems of thermal management to achieve high precision are always underestimated and are much more difficult to solve effectively when the design is almost finished.
- The limited hardware performance of the FGC ADCs has been improved 3-5 times over a limited temperature range by a digital correction algorithm.

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