CURRENT MONITOR FOR THE ISIS SYNCHROTRON RF CAVITY BIAS REGULATOR

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Abstract

The ISIS facility at the Rutherford Appleton Laboratory in the UK is currently the world's most intense pulsed neutron source. The accelerator consists of a 70 MeV H^- linac and an 800 MeV, 50 Hz, proton synchrotron. The synchrotron beam is accelerated using six, fundamental harmonic, ferrite loaded, RF cavities each having its own high voltage RF drive amplifier and bias system. Each of these RF cavities is driven as a high Q tuned RF circuit; the resonant frequency being controlled by passing a current through a bias winding. This current comes from the cavity's own Bias Regulator system which consists in part of eight banks of 10 transistors.

The machine is currently being upgraded by adding four second harmonic cavities, each having its own drive amplifier and bias system. The second harmonic bias regulators have eight banks of 40 transistors (i.e. four transistors in parallel to replace each of the 10 single ones used in the original system).

This paper describes the design of a modular system which will use digital techniques to monitor and display the current of each of the 80 transistors in the Fundamental Bias Regulator system, or 320 transistors in the Second Harmonic System.

INTRODUCTION

The layout of a fundamental bias system is shown in Figure 1 below. The Bias Regulator consists of 8 banks of 10 transistors, giving a total of 80 transistors per system that need to be individually monitored (this rises to 320 for the second harmonic system).

The function of the bias system is to drive a precisely controlled current waveform through the bias winding of an RF cavity. During the 10ms acceleration period this biasing current is swept from 300 to 2300A causing the resonant frequency to vary from 1.34 MHz to 3.09 MHz (2.68 MHz to 6.18 MHz for the second harmonic system). A further 10ms is taken to drive the biasing current back down to 300A ready for the next acceleration pulse. The Bias Regulator waveform is shown in Figure 2.

The main complexity of the current monitoring system is that the ground lines of the transistors are connected to the emitter busbar and not to earth. Therefore the emitter

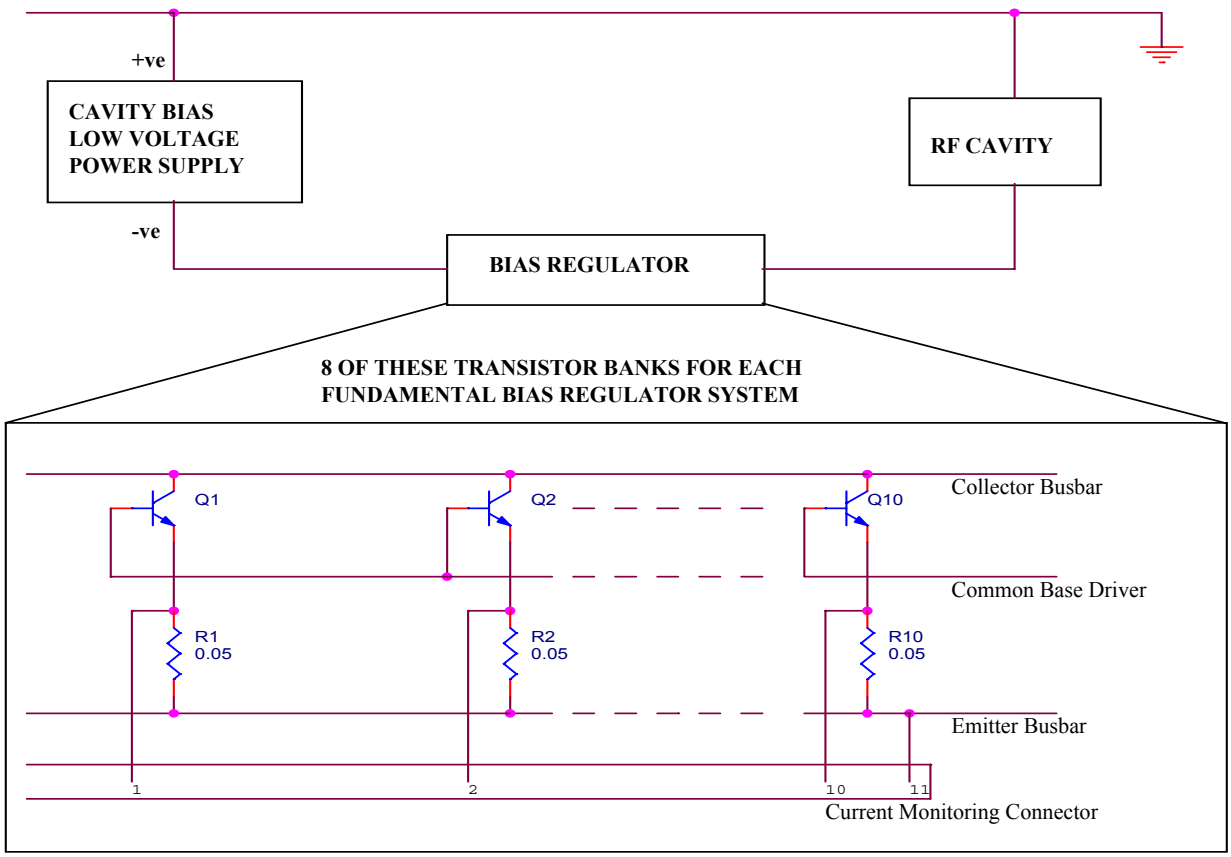

Figure 1: Fundamental Bias Regulator System.

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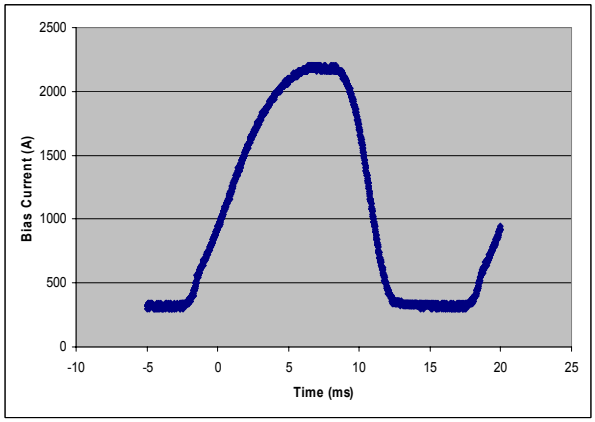

Figure 2: Bias Regulator Current Waveform.

busbar has to be used as the negative reference for the front end of the circuit.

SYSTEM REQUIREMENTS

The requirements for this system are that the current on any of the 80/320 transistors in the bias regulator can be read at any point during the 20ms cycle, and displayed digitally on the front panel of the control crate. In order to facilitate this a minimum of three inputs are required:

- The number of the transistor to be read
- The bank in which the transistor is located
- Point of sample in the cycle (in ms)

These will all be selectable from the front panel.

An addition to these requirements will be the ability to do a sweep of current readings over the entire waveform on one transistor, or on a bank of transistors.

INITIAL INVESTIGATIONS

Analogue to Digital Converters (ADC)

From Figure 1 it can be seen that the current on each transistor is read via the voltage drop across the 0.05Ω resistor between the transistor emitter and the emitter busbar. In the fundamental system the current range per transistor will be 3.75 to 27.5A, which results in a range of 0.1875 to 1.375V at the Current Monitoring Connector (the second harmonic system has 0.22Ω resistors in the emitter circuit, giving approximately the same voltage drop). In order to process this digitally an ADC is required that is capable of accepting such a voltage range and whose ground line can be connected to the emitter busbar.

At the outset it was decided that a multiplexing ADC would be required with a minimum of 8 analogue input channels. The first choice of ADC was not successful due to clocking and Serial Peripheral Interface (SPI) communication problems when combined with the microprocessor. These problems were solved in part by using interrupts and clock dividers but this was deemed not to be a very robust solution.

The chip used in the final design, LTC1290, solved these problems and gave a higher resolution of 12 bits instead of the original 8 bits. It significantly simplified the interface with the microprocessor and allowed a much faster throughput of data, being fully duplex, with a shift clock frequency (f_{SCLK}) of 2MHz and an A/D clock frequency (f_{ACLK}) of 4MHz [1]. This resulted in a cycle time of:

$$t_{cycle} = 12/f_{SCLK} + 56/f_{ACLK} = 6\mu s + 13\mu s = 19\mu s$$

The only complication with this ADC is that its full duplex serial interface outputs the previous conversion value while reading in the next cycle setup data – this can lead to sequencing issues, so careful timing and data-ready asserts are required within the processor.

Isolation

As the measurements will be taken with reference to the emitter busbar and not to ground, isolation is required between the data acquisition point and the processing point. Therefore opto-isolators are used on all the inputs and outputs of the ADC. Clearly in order to keep this isolation the ADCs cannot be powered from the same place as the processing device so each group of five ADC's is powered by an isolated DC-DC converter.

PIC v's PLD

It was originally intended to implement the system using a microcontroller, namely the PIC16F88 from Microchip. This was due to familiarity with such chips, their development environment, and ease of access to a development board. The initial investigations involved trying to interface the PIC with the multiplexing ADC. As mentioned previously this gave significant problems due to the required clocking for the ADC not being synchronised with that of the PIC and as a result the ADC appeared to lose data off the end of conversions.

Once the ADC was changed to the LTC1290 the interface with the PIC became much simpler due to the full duplex communication, and the issue with the readout from the ADC being one cycle behind the input was taken care of by issuing the read instruction twice every cycle. A prototype was built using these chips and its functionality rigorously tested. At this point the question arose about reusability and the possibility of increasing the specification.

It was clear that the PIC would soon be operating at the limit of its capabilities and perhaps moving to a Programmable Logic Device (PLD), such as a Field Programmable Gate Array (FPGA) or Complex Programmable Logic Device (CPLD) would provide a more useful and faster system for the future.

A second-generation in-system programmable CPLD, the ispLSI5512VE from Lattice [2], was chosen. It has 512 registers and 256 I/O pins so is more than capable of processing the maximum amount of data in the system. The CPLD is programmed in-system using VHSIC

Hardware Description Language (VHDL). Along with the code change, came a change of development environment to the ispLEVER® programming environment from Lattice - this environment allows full simulation of the digital circuit before programming the device.

CURRENT DESIGN

The final system design consists of one control board and front panel per bias regulator system, combined with two daughter boards for the fundamental systems, and eight for the second harmonic systems. The daughter boards will be mounted away from the main control crate on each of the banks of transistors. Figure 3 shows a block diagram of the system with only one daughter board attached.

The front panel has a digital display for the current output and the following user selectable inputs:

- Bank select
- Transistor select
- Time delay required

The control board houses the PLD and associated I/O and power circuitry, while the daughter boards have five multiplexing ADCs each giving a total of 40 channels per board. The daughter boards also contain some logic elements which allow the result from the correct channel to be fed back to the PLD rather than having eight output lines from each daughter board returning to the control board.

Within the PLD there are three main entities that process the data:

- Timing_Counter – takes in the time delay from the front panel and uses it to ensure that the current waveform is sampled at the correct time within the cycle.
- Transistor_Select – translates the transistor select input into the correct chip and channel to be sampled. This is then sent to each of the daughter boards, resulting in the same chip and channel being sampled on every board.
- Current_Calculator – uses the bank select input to decipher which board to read back from. It then clocks in the serial output from the correct daughter board. A look-up table is used to identify the correct current value corresponding to this measured input voltage. The current value is subsequently displayed on the front panel.

RESULTS

The first set of boards for this system have been manufactured and tested with only minor modifications required. The VHDL entities mentioned above have been written and successfully simulated, but further work on their interfacing is required. The only outstanding item is the front panel, which will be designed and manufactured this autumn. Once this is complete the system can be installed on the test-rig and pre-commissioning tests carried out.

REFERENCES

[1] http://www.linear.com/pc/downloadDocument.do?navId=H0,C1,C1155,C1001,C1158,P1594,D2494
[2] http://www.latticesemi.com/lit/docs/datasheets/cpld/5512ve.pdf

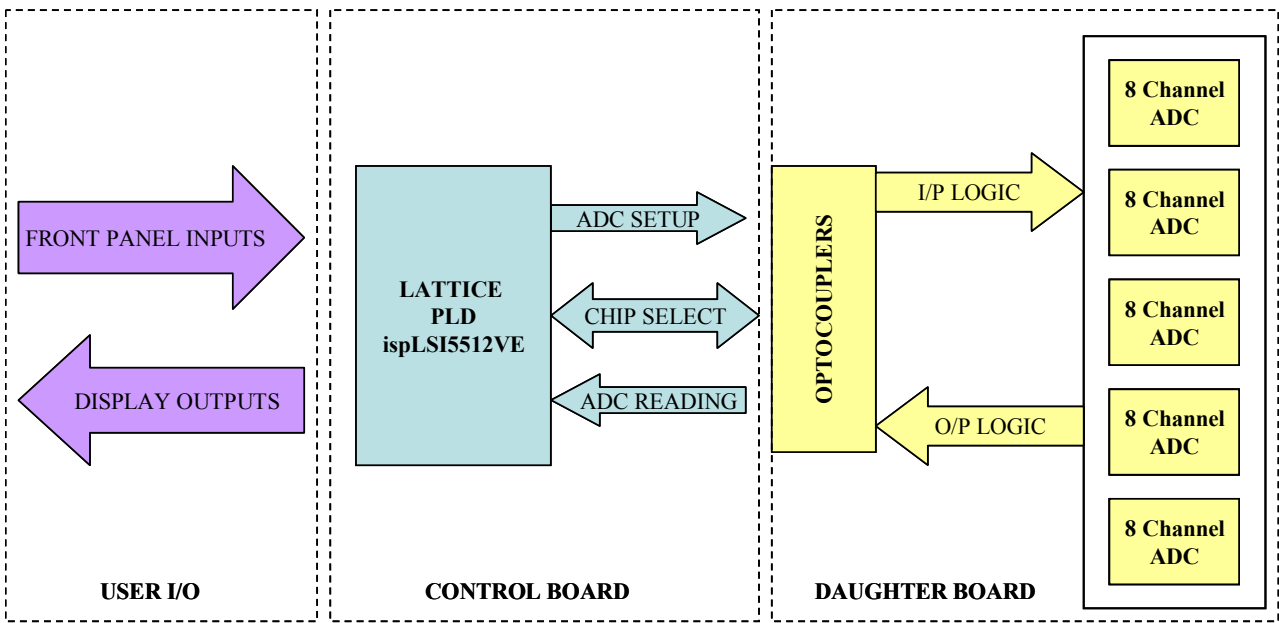

Figure 3: Block Diagram of Current Monitor System.

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