FPGA BASED ILC CAVITY SIMULATOR

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Abstract

This paper presents a FPGA based Real Time Simulator of ILC superconducting RF cavities. The system has been developed on a Lyrtech VHS-ADAC board, through the use of Xilinx System Generator and Simulink.

This FPGA system is mainly being developed for allowing testing of the LLRF systems in the real time and for different cavities parameters.

INTRODUCTION

In the International Linear Collider the beam will be accelerated using superconducting RF cavities. For guarantying the focusing of the beam, it is important to maintain constant the amplitude and the phase of the fields inside these cavities.

And it is the Low Level RF (LLRF) control system which plays this important role of maintaining the proper phase and amplitude information for the RF field inside the superconducting cavities. But the high operational overhead of the high power cryogenic hardware and the risk of its damage during the control hardware tests make it necessary to have a LLRF test bed independent of the real hardware. Thus, we have developed this Real Time Simulator (RTS), which will be useful for the testing and commissioning of the Low Level RF control system, including the exception handling capabilities, and possibly as a noiseless behavioral reference for each cryomodule during operation.

CAVITY MODEL

The cavity model used in the simulator is based on the analysis made by Thomas Schilcher in [1]. The idea is to describe the cavity through its electrical equivalent circuit, which is a selective resonator typically described by an RLC parallel circuit (see Fig.1).

Another important effect such as the Lorentz Detuning can be described by another set of equations – the mechanical model – which are coupled to the electrical model equations through the detuning constant, as it will be explained more in detail.

Electrical and Mechanical Model

The electrical properties of the cavity are described by the following set of equations:

$$\dot{V}_r + \omega_{1/2} \cdot V_r + \Delta\omega \cdot V_i = R_L \cdot \omega_{1/2} \cdot I_r$$

$$\dot{V}_i + \omega_{1/2} \cdot V_i - \Delta\omega \cdot V_r = R_L \cdot \omega_{1/2} \cdot I_i$$

(1)

Where Vr and Vi are respectively the real and the imaginary part – amplitude and phase – of the field inside the cavity. The other parameters in equations (1) are summarized in the table 1.
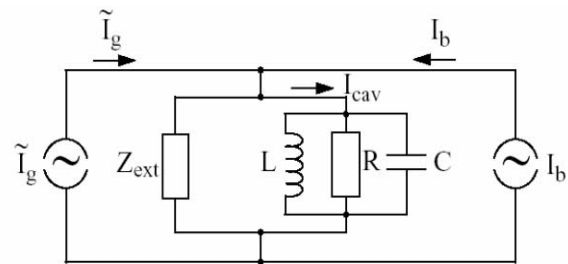

Figure 1: Electrical model of the cavity

The mechanical properties of the cavities are described by another set of differential equations, whose variable is the total detuning Δω which appears in the Eq. 1 and 2.

Table 1: RTS Parameters

Cavity simulator parameters	Values
Resonance Frequency	1.3 [GHz]
Loaded quality factor - **Q**	**Adjustable via software interface**
Shunt resistance	500***Q** [Ω]
Total detuning	Described by the mechanical model set of differential equations

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CAVITY DISCRETE MODEL

The first step to the implementation of the cavity model in the FPGA is transforming the previous equations into a discrete form. For doing that, the method chosen was the Euler forward methods, which lead to the following equations:

$$V_r(n) = [1 - \omega_{1/2} \cdot \Delta t] \cdot V_r(n-1) - \Delta \omega \Delta t \cdot V_i(n-1) + R_L \cdot \omega_{1/2} \cdot \Delta t \cdot I_r$$

$$(2)$$

$$V_i(n) = [1 - \omega_{1/2} \cdot \Delta t] \cdot V_i(n-1) + \Delta \omega \Delta t \cdot V_r(n-1) + R_L \cdot \omega_{1/2} \cdot \Delta t \cdot I_i$$

From the equations above, constructing the simulator appears straightforward: the value at the nth instant is the value at the previous instant elaborated through multipliers and adders. And with the use of Sysgen and Simulink, the implementation of the block diagrams and the generation of hardware code is quite simple since it allows an higher level of abstraction compared to the use of VHDL. A block diagram implemented in Simulink is shown if fig.2
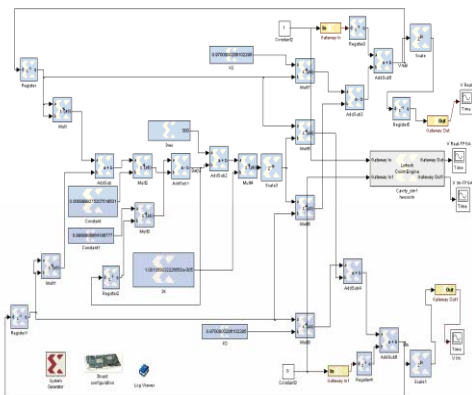

Figure 2 : A Simulink cavity block diagram

IMPLEMENTATION

The RTS has been implemented on a Lyrtech VHS-ADAC board, which provides 8 ADC/8 DAC channels and a Xilinx Virtex-II FPGA. The latest has been programmed through the use of Xilinx System Generator on Simulink, which significantly simplified the creation of HDL code.

Xilinx System Generator for DSP is a plug-in to Simulink, which enables designers to develop high performance DSP systems for Xilinx FPGAs. The tool automatically generates synthesizable Hardware Description Language (HDL) code mapped to Xilinx pre-optimized algorithms. As a result, from an abstract representation of a system-level design, the tool easily transformed this single source code into a gate-level representation.
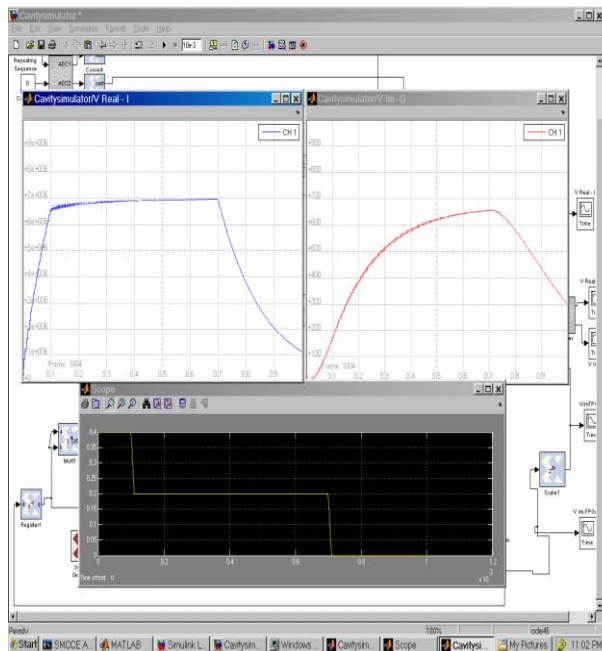

Figure 3: Results of simulations on Simulink

RESULTS OF THE SIMULATIONS

Two cavities have been successfully implemented, and some results of the simulations can be seen in fig.3, where the I and Q components (in phase and in quadrature) of the vector field are plot, when the input to the cavity is the 'fill-flattop-empty' signal. The simulator has been implemented using the 64-bit fixed point arithmetics with 40-bits fractional part. The maximum clock frequency is above 30 MHz and the overall latency is around 500 nsec (about 10 clock cycles to complete the simulation). The total FPGA occupancy is 10%. A simulation connecting the RTS to the SIMCON 3.1 LLRF board has also been successfully performed recently at FNAL. Soon more effects will be included in the real time simulator, in particular all of the effects so far included in the PVC [2].

REFERENCES

[1] Thomas Schilcher, "Vector Sum Control of Pulsed Accelerating Fields in Lorentz Force Detuned Superconducting Cavities," Ph.D. Thesis, University of Hamburg, (1998).

[2] Justin Keung, PVC - http://einstein.hep.upenn.edu/~keungj/simulation.html

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