SLOW KICKER MAGNET SYSTEM WITH ENERGY RECOVER PULSE POWER SUPPLY WITH EXTENDED FLAT TOP

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Abstract

Danfysik has developed a novel Slow Kicker Magnet Power Supply ERMPPS (Energy Recover Magnet Pulsed Power Supply) with associating magnet achieving high stability, long flat top and low energy consumption. Two Slow Kicker Magnet Systems have been built to Rutherford Appleton Laboratory (RAL), one low and one high current supply. The magnets are laminated window frame type. The ISIS synchrotron at RAL produces high energy proton bunches at 50 Hz rate. The Slow Kickers operate at 10 Hz, directing a portion of the extracted protons to a second beam line. The flat top width is 600 µsec with a flat top and peak-peak stability better than 100 ppm. The rise and fall times are 12 msec.

The power supply has been developed having following highlights:

High accuracy with adjustable output current from nearly zero, wide range setable flat top width and rise time, energy recovery, digital flat top and rise time regulation loop in FPGA and variable repetition frequency down to one shot operation. The flat top width and rise time settings are bounded by the actual load and internal component values.

INTRODUCTION

The pulsed magnet power supply is designed to produce a half sine profile current with a rise time of 12 msec a flat top duration of 600µsec and flat top linearity and stability of 100ppm. All three parameters 'rise time', 'flattop width' and 'flatness' are digitally adjustable.

Two ERMPPS have been constructed, one with a peak current of 2800A using a 1300V charging voltage and one 450A with a charging voltage of 220V.

Both power supplies are connected to the same magnet type having a load inductance of 3.7mH

The pulsed magnet power supply design is based on a standard Danfysik System 8500 MPS control concept with a dedicated output design converter and two digital regulation loops.

This paper reviews the power converter topology, the digital regulation principle and the magnet construction. Also performance measurements electrical as well as magnetic are presented.

POWER SUPPLY BLOCK SCHEMATIC

Figure 1 shows the power supply block schematic. As indicated the power supply is divided into three major blocks: Input and output converter and a control electronic block. The input converter is constructed in a standard way, and will therefore not be addressed further in this paper. The Control Electronic block is build around a standard Danfysik System 8500 control module with a dedicated digital regulation module. Only the digital regulation module will be addressed further in this paper.

Output converter

The output converter can be divided into three sub converters, a high and a low voltage capacitor charger and the actual power converter which mainly consist of IGBT switches.

The LV (Low Voltage) & HV (High Voltage) capacitor charge converters are build upon Danfysik's type 859 current controlled switch mode topology, which can be configured in numerous ways capable of handling currents up to 3000A and voltages up to 1300V in one, two or four quadrant operation. In this application a buck converter configuration has been chosen for the LV charge supply and a boost converter for the HV converter. The connection to the regulation module is realized with optical fibres to ensure a 5KV isolation barrier.

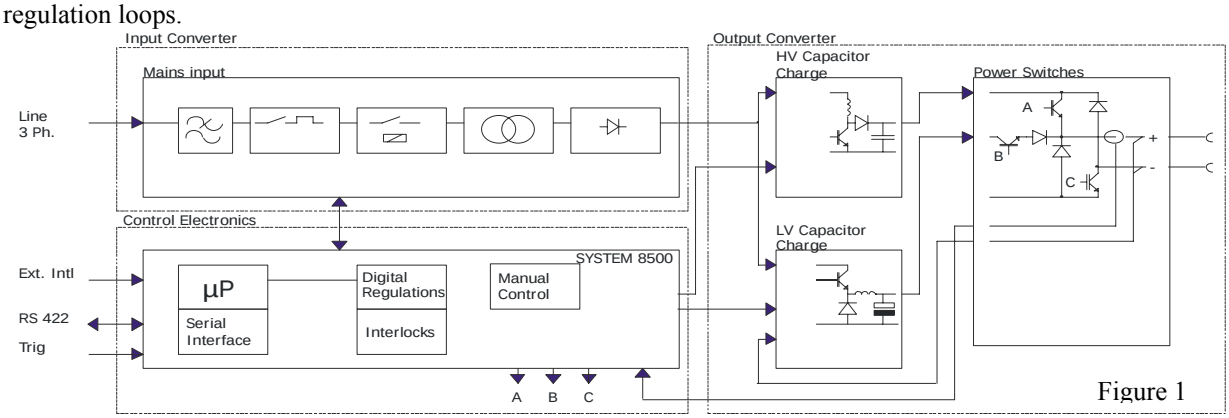

Figure 1

The tables below shows key data for the two power supplies: K1 and K2.

Given

	K1	K2
Iout	450A	2800A
Load L	3.70mH	3.70mH
Load R	19.60mΩ	19.60mΩ
Internal R	2.50mΩ	1.00mΩ
Load Cable	18.00mΩ	7.50mΩ
Rise time	12ms	12ms
Flat Top Accuracy	25ppm	25ppm
Flat top time	600µSec	600µSec
Repetition time	100ms	100ms
Eddy Loss Iron	8.0W	50.0W
Eddy Loss copper	0.5KW	2.9KW

Table 1a

Data

	K1	K2
HV Cap	22mF	22mF
LV Cap	0.7F	1.7F
HV Val Start value	220V	1277V
LV Val Start value	27V	88V
LV Power	1201W	25.4KW
HV Power	770.3W	13.1KW
HV peak Chrg. curr.	4.3A	12.2A
LV peak Chrg. curr.	45A	289A

Table 1b

(The 25 ppm accuracy is a design goal.)

The 'Power Switch' block transfers the stored capacitor energy to and from the load. Its working principle is as follows:

When the capacitor voltages are charged to their specified values, a ready signal is generated to the control electronic. Issuing a trigger signal hereafter either from a remote source or a local test push button will start the pulse sequence. First IGBT A & C are turned ON forming a resonant circuit between the magnet and the HV capacitor. The flat top period begins when the output current measured reaches the desired set value. At this point "IGBT A" will be turned OFF and the magnet current will hereafter flow through IGBT B and the low voltage diode. After the 600µs flat top duration "IGBT C" is turned OFF initiating the recovery period recovering the magnet energy back to the HV capacitor through C's top diode.

The flat top accuracy is achieved from following principle: If the DC flat top voltage (LV capacitor voltage) is the same as the re load resistance times the current, the voltage across the load inductance will be zero. No voltage across an inductor is the same as no current change:

$$\Delta I = 1/L * \int V_L dt$$

If V_L is zero will ΔI is also zero.

IGBT B can be used to achieve even higher accuracy if coupled in a linear voltage controlled mode, or be omitted if the LV may be applied during the OFF state.

Regulation module

The working principle of the regulation module is as follows:

On receipt of a new set current the FPGA predicts a new set of HV and LV values suitable for the desired current pulse. A trigger signal will force IGBT A & C ON and simultaneously start the 'rise time' timer. When the output current equals the set value 'IGBT A' is turned OFF, the 'rise time' timer value is sampled and the output current is measured (1st). The flat top timer with a pre programmed length is started, and at the end of the period the output current is measured again (2nd) sampled, and the recovery period is initiated (see previous paragraph).

The difference between the sampled 'rise time' value and the rise time set value is passed to the PI regulation loop inside the FPGA. If the rise time is short, the HV is increased at the next pulse and visa versa.

The difference between the first measured output current, which should be equal to the set current value, and the second measured output current added with a desired slope is passed to the PI regulation loop inside the FPGA regulating the pulse flatness. If difference is negative, the LV is increased according to the regulation PI constants.

The added desired slope compensation is used, if the desired flat top current is not 100% horizontal. Due to time constants and Eddy currents in the magnet, the field will not follow the current exactly but lack a bit behind. Programming a negative current slope will therefore result in a much better field top.

The PI constants of both regulation loops can be set to a best optimum through a direct RS422 line connected to the FPGA.

The achieved resolution is:
Current setting resolution: 16ppm
Rise time resolution: 10µsec
Flat top resolution: 2ppm

Figure 2 on the next page shows the block schematic of the FPGA regulation loop.

FT = Flat Top
RT = Rise Time

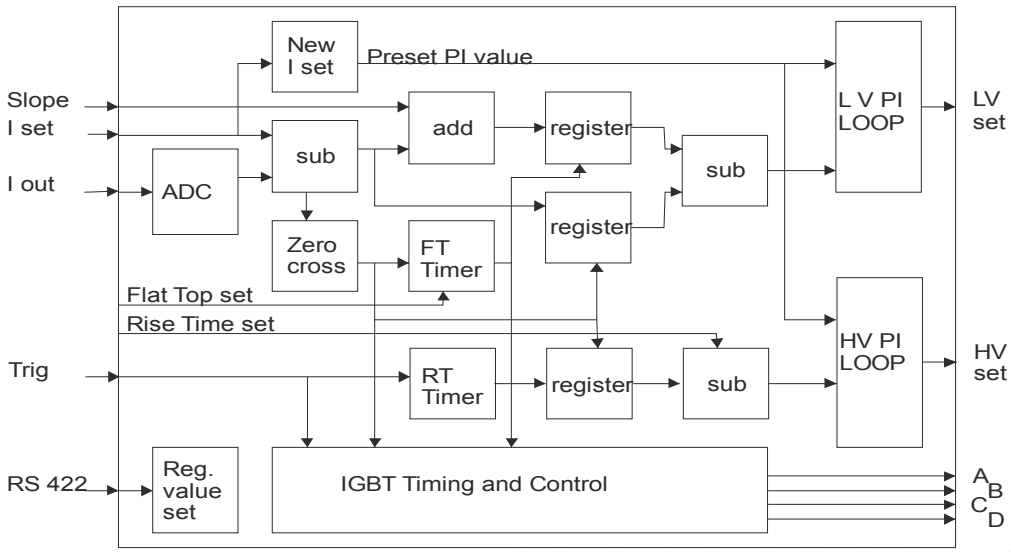

Figure 2: FPGA regulation loop

SLOW KICKER MAGNET

The magnet is a laminated window frame type with an aperture gap of 220 mm and a magnetic length of 500 mm. The integrated magnetic field is proven to fulfil requirements concerning homogeneity within 0.25% in an area of 180 x 160 mm (w x h) and stability under ramped condition. The magnet field is 0.864T @ 2800A.
Figure 3 shows a picture of the magnet.

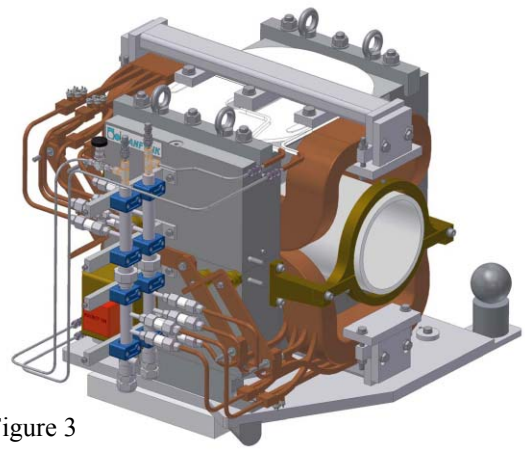

Figure 3

TEST RESULT

Following are three test records shown.

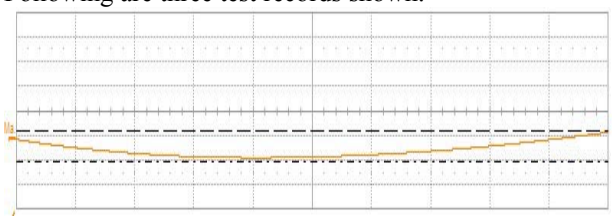

Figure 4

Magnetic flattop field integral, compensated current.
Resolution: 50µs and 80ppm per division

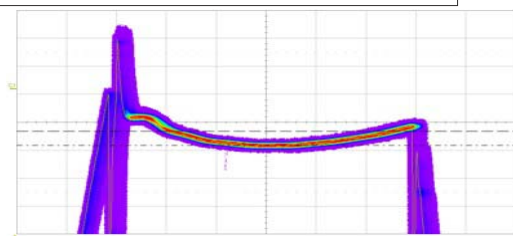

Figure 5

8 hours current stability test @ 2800A.
Resolution: 100µs and 100ppm per division.

The first spike is due to the 50metre of cable and the cable matching filter. The saddle shape is due to eddy currents in the magnet.

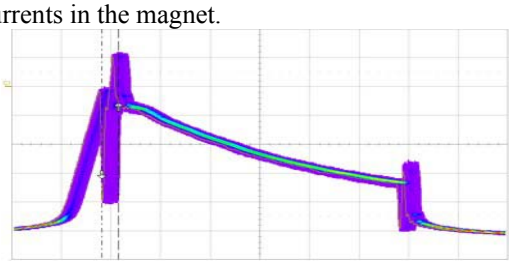

Figure 6

8 hours current stability test with magnet compensation.
Resolution: 100µs and 200ppm per division.

CONCLUTIONS

The novel Slow Kicker ERMPPS design has proven to fulfil the tight specification, easy to use and adjust with an excellent efficiency. This enabling a superb matching to the attached magnet and compensating for its parasitic components. All providing an extended flat top duration, within a high accuracy in both the top flatness and the timing without the magnet temperature influence. This due to the double digital regulation loops.