

DEVELOPMENT OF DIGITAL LOW-LEVEL RF CONTROL SYSTEM USING MULTI-INTERMEDIATE FREQUENCIES

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Abstract

In a superconducting accelerator, an FPGA-based low-level rf system is adopted and a digital feedback control system is utilized to satisfy the requirement of stability in the accelerating field. A digital low-level rf system using multi-intermediate frequencies has been developed and the stability of the feedback operation is estimated using a cavity simulator based on an FPGA board. In this study, the rf system is examined and the results of estimations that are obtained using the cavity simulator are reported.

INTRODUCTION

Superconducting accelerators require accelerating phase stabilities ranging from 1° to 0.01° and amplitude stabilities ranging from 1% to 0.01% at the operating frequency. In order to satisfy these requirements, vector sum feedback (FB) and feedforward (FF) control are adopted for rf control and a digital low-level rf (LLRF) system based on an FPGA/DSP board has been developed. In the digital LLRF control system, an rf probe signal picked up from a cavity is down-converted to an intermediate frequency (IF), while preserving the amplitude and phase information of the rf signal. The IF signal is sampled by an analog-to-digital converter (ADC) with a constant sampling ratio.

For vector sum FB control, the number of ADCs required for field detection is equal to the number of cavities, as shown in Figure 1(a). In the superconducting accelerator, one klystron provides power to many (more than 20) cavities. It is difficult to construct an FPGA board that holds such a large number of ADCs because the number of lines between the FPGA and the ADCs is large.

In order to decrease the number of ADCs used for field detection, a digital LLRF control system using a new (IF-mixture) technique is under development, as shown in Figure 1(b). As shown in Figure 2, rf signals from a cavity are down-converted to a different IF frequency and the IF signals are combined by a combiner in the digital

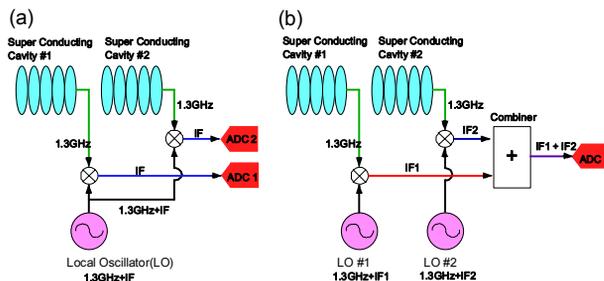


Figure 1: Schematic diagram of the digital LLRF system: (a) conventional and (b) IF-Mixture technique.

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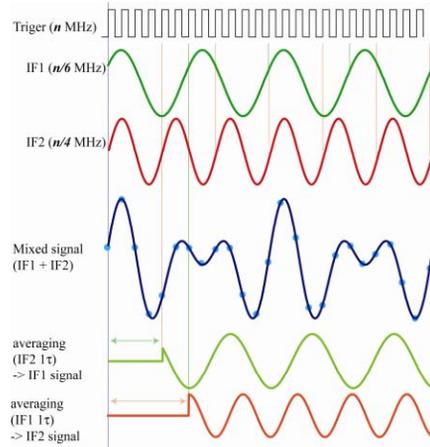


Figure 2: Concept of IF-mixture technique. By digital processing, two IF signals are restored.

LLRF system. The combined IF signal is detected with an ADC and returned to the original IF signals by digital signal processing. In a two-IF frequency system, we can reduce the number of ADCs by half.

IF-MIXTURE TECHNIQUE

The down-converted IF signal is expressed as follows:

$$x(t) = I(t) \cdot \cos(\omega_{IF}t + \varphi) + iQ(t) \cdot \sin(\omega_{IF}t + \varphi)$$

where $I(t)$, $Q(t)$, and φ are the I and Q components and the loop phase of the cavity, and $\omega_{IF} = 2\pi \cdot IF$. In the IF-mixture technique, the sampling ratio of an ADC and the frequencies of the IF signals must fulfill the condition $IF = (M+1/N)SR$, where SR is the sampling ratio of the ADC, M is an integer, and N is an integer greater than 3. In this experiment, we choose 40.625 MHz as the sampling ratio of the ADC and $(M, N1, \text{ and } N2) = (0, 6, \text{ and } 4)$.

The combined IF signal is expressed as

$$\begin{aligned} x_1(t) + x_2(t) &= I_1(t) \cdot \cos(\omega_{IF1}t + \varphi_1) + iQ_1(t) \cdot \sin(\omega_{IF1}t + \varphi_1) \\ &\quad + I_2(t) \cdot \cos(\omega_{IF2}t + \varphi_2) + iQ_2(t) \cdot \sin(\omega_{IF2}t + \varphi_2) \end{aligned}$$

In the case of a superconducting cavity, the $I_i(t)$ and $Q_i(t)$ signals change slowly and are regarded as the constants I and Q during the period $1/IF$. After sampling at the ADC, this combined IF signal sequence is represented as

$$\begin{aligned} x_1(n) + x_2(n) &= I_1 \cdot \cos\left(\frac{2\pi}{N_1} \cdot n\right) + iQ_1 \cdot \sin\left(\frac{2\pi}{N_1} \cdot n\right) \\ &\quad + I_2 \cdot \cos\left(\frac{2\pi}{N_2} \cdot n\right) + iQ_2 \cdot \sin\left(\frac{2\pi}{N_2} \cdot n\right) \end{aligned}$$

The combined IF signal sequence is averaged along with $N1$ or $N2$ consecutive signal samples to restore the signal sequences $x_1(n)$ and $x_2(n)$. By using following formula

$$\sum_{n=1}^N \left(\frac{\sin}{\cos} \right) [(n-1)\theta] = \frac{\sin \frac{N\theta}{2}}{\sin \frac{\theta}{2}} \left(\frac{\sin}{\cos} \right) \left[\frac{(N-1)\theta}{2} \right]$$

where θ is the phase advance between two consecutive samples ($\theta = 2\pi/N$), the calculated result is expressed as

$$X_1(n) = \sum_{n=1}^{N_2} (x_1(n) + x_2(n)) = \frac{\sin \frac{N_2\theta_1}{2}}{\sin \frac{\theta_1}{2}} \cdot x_1(n)$$

$$X_2(n) = \sum_{n=1}^{N_1} (x_1(n) + x_2(n)) = \frac{\sin \frac{N_1\theta_2}{2}}{\sin \frac{\theta_2}{2}} \cdot x_2(n)$$

where $X_1(n)$ and $X_2(n)$ are restored $x_1(n)$ and $x_2(n)$, respectively. The constant phase shift caused by averaging is ignored in this calculation.

The I and Q components of each IF signal can be numerically calculated by using the following equation for averaging consecutive signal samples [1].

$$I = \frac{2}{N} \sum_{n=1}^N x_i(n) \cos\left(\frac{2\pi}{N} \cdot n\right)$$

$$Q = \frac{2}{N} \sum_{n=1}^N x_i(n) \sin\left(\frac{2\pi}{N} \cdot n\right)$$

In the IF-mixture technique, the delay time for forming the I and Q components from the combined IF signal is $(N1 + N2)/SR$ and become larger in comparison with the conventional technique. However, it is expected that the averaging of the samples reduces the influence of noise and jitter caused by the ADC sampling.

DIGITAL FEEDBACK SYSTEM

The system configuration for employing the IF-mixture technique consists of an FPGA board developed for the KEK-STF, two cavity simulators, and a signal distribution system, as shown in Figure 3 [2, 3]. The FPGA board

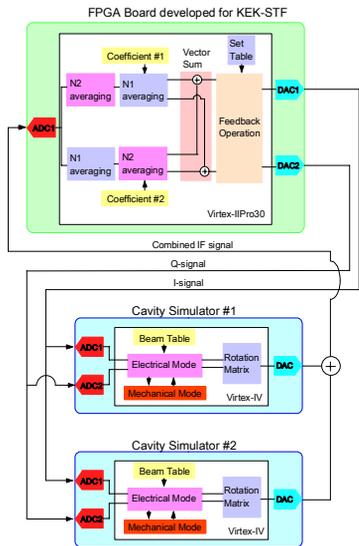


Figure 3: Schematic of system configuration.

consists of an FPGA chip (VirtexIIPro30), ten 16-bit ADCs (LTC2204), and two 14-bit DACs (AD9764). The DACs are mounted on the FPGA board output I and Q signal and are connected to the ADCs of the cavity simulators. These cavity simulators constructed with a commercial FPGA board (Xilinx, Xtreme DSP Development Kit-IV, an FPGA chip (Virtex-IV), two 14-bit ADCs (AD6645), and two 14-bit DACs (AD9772A)) are operated with a frequency of $4 \times IF$ and the cavity signal is estimated by calculating the state equation of the cavity in a discrete form [4]. The DAC of the cavity simulator outputs the cavity signal modulated with the IF frequency. In this experiment, these two cavity simulators are operated with different clock signals and the IF signals are combined with a combiner (Mini-circuits, ZFSCJ-2-1). The combined IF signal is sampled by the ADC on the FPGA board with a constant sampling ratio.

Signal Distribution System

In this digital FB system, three kinds of clock signals are utilized: clock signals for the FPGA board the cavity simulators #1 and #2. The signal distribution system consists of an RF&CLK unit developed for the KEK-STF and three evaluation boards containing programmable clock distribution ICs (AD9510/PCB); the system feeds a 40.625-MHz clock signal to the FPGA board and cavity simulator #1 and a 27.083-MHz clock signal to cavity simulator #2, as shown in Figure 4. Figure 5 shows the frequency spectrum of the combined IF signal, which is obtained using the cavity simulator.

FEEDBACK PERFORMANCE

The performance of the digital FB system using the IF-mixture technique is evaluated using the cavity simulators. Figure 6 shows the result at the set point of 16,000 under P control for the gain of 80 (without FF). As shown in Figure 6, the feedback loop of the system is closed and

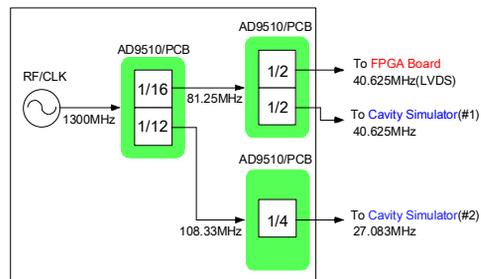


Figure 4: Schematic of signal distribution system.

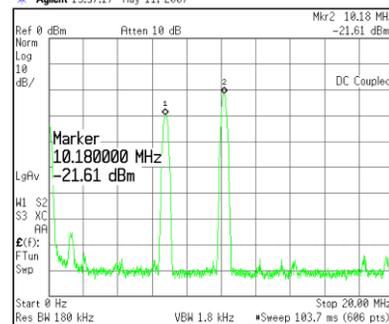


Figure 5: Frequency spectrum of combined IF signal.

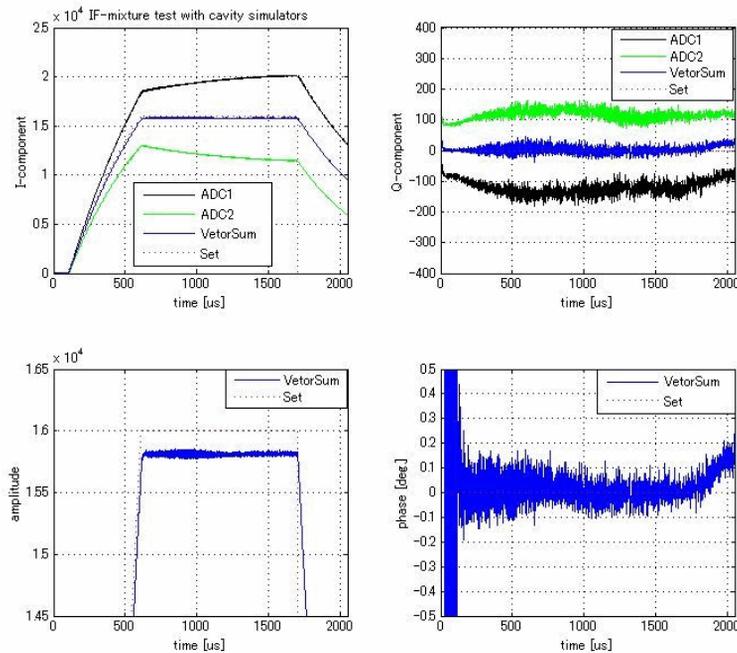


Figure 6: Measured I/Q and amplitude/phase components with FB operation.

the signals of the cavity simulators #1 and #2 are separated from the combined IF signal. The corresponding errors in the amplitude and the phase are 0.11% (RMS) and 0.05° (RMS), respectively.

Figure 7 shows the relation between the P-gain and the amplitude and phase stabilities at flat top from 650 to 1650 us. The P-gain is calculated by the difference between the set point and the average of the measured flat top. The FB operation becomes unstable at a P-gain greater than 90. In the region of stable FB operation, the errors in the amplitude and phase are 0.1% (RMS) and 0.04° (RMS), respectively. These stabilities satisfy the limits of RF field stabilities (less than 0.3%, 0.3°) in KEK-STF phase 1.

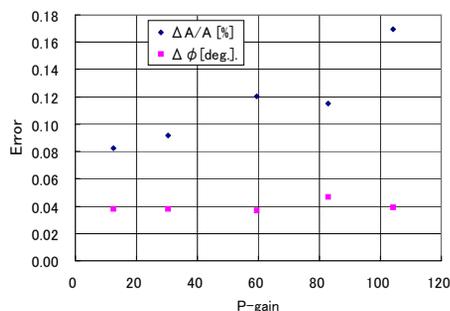


Figure 7: Errors in amplitude and phase at flat top.

FUTURE PLAN

In this experiment, two-IF signals are combined and the information pertaining to the I and Q components of each IF signal is separated. Now, we are planning to combine three or more IF signals. When three IF signals with the combination (N1, N2, and N3) are combined, the step

needed for calculating the I and Q components using the filtering used in this technique is $(N1N2+N3)$. In order to suppress the delay time, we must choose a higher sampling ratio for the ADC.

At KEK-STF phase 1, a total of eight superconducting cavities will be operated. In order to demonstrate the IF-mixture technique using a superconducting cavity, the signal distribution system will be modified to generate the local frequency (LO) signal.

SUMMARY

A digital FB system using the IF-mixture technique on two IF signals has been developed. The system is examined by employing two cavity simulators and shows stabilities of 0.1% (RMS) and 0.04° (RMS) for the amplitude and phase, respectively. The demonstration of the IF-mixture technique by using three IF signals and the superconducting cavity in KEK-STF phase 1 is planned.

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