DEVELOPMENT OF THE PEFP LOW LEVEL RF CONTROL SYSTEM*

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Abstract

The RF amplitude and the phase stability requirements of the LLRF system for the PEFP (Proton Engineering Frontier Project) proton linac are within 1 % and 1 degree, respectively. As a prototype of the LLRF, a simple digital PI control system based on commercial FPGA board is designed and tested. The main features are a sampling rate of 40 MHz which is four times higher than the down-converted cavity signal frequency, digital in-phase and quadrature detection, pulsed mode operation with the external trigger, and a simple proportional-integral feedback algorithm implemented in a FPGA. The developed system was tested with 3 MeV RFQ and 20 MeV DTL, and satisfied the stability requirements.

INTRODUCTION

In the 100 MeV proton linear accelerator for PEFP, the RF source will power an RFQ cavity and DTL tanks operated at a frequency of 350 MHz [1]. The low level RF(LLRF) system for 100 MeV proton linear accelerator provides field control including an RFQ and DTL tanks at 350 MHz. In our system, an accelerating field stability of ±1% in amplitude and ±1 deg. in phase is required for the RF system. The digital RF feedback control system using the FPGAs and PowerPC Embedded Processor is adopted in order to accomplish these requirements and flexibility of the feedback and feed-forward algorithm [2]. The analog front-end also developed which contains the IQ modulator, RF mixer, attenuators etc. To check the performance of the digital feedback control system, low power test with a dummy cavity has been performed with an intentional perturbation and has shown that the feedback system rejected the perturbation as expected. High power RF test with 3 MeV RFQ and 20 MeV DTL has been performed and the accelerating field profiles were measured and the pulse-to-pulse stability was checked by pulse operation with 0.1 Hz repetition rate. The detailed LLRF system description and test results are given in this paper.

LLRF SYSTEM DESCRIPTIONS

The hardware components can be divided into the analogue parts and the digital parts. The analogue parts mainly deal with the signal mixing, IQ modulation and interlock system and the digital parts contain the control algorithm. The analogue parts consist of various components such as IQ modulator (Analog Devices AD8345), RF mixer, RF switch, RF amplitude detector, phase comparator and VSWR trip circuit along with many attenuators and power splitters. All of the analogue components are installed in the 19” subrack. A 350 MHz cavity field pick-up signal is converted to 10 MHz IF signal by mixing the 340 MHz IF signal. The amplitude and phase of the cavity field can be measured by RF detector and phase comparator; therefore it is possible to compare the RF amplitude and phase measured by analogue system with those measured by digital system. The VSWR trip circuit and interlock system protect the machine in the event of an arcing or an RF full reflection.

The main hardware components of the digital RF feedback system are ADC for sampling of the RF signal, FPGA for the signal processing and DAC for driving the IQ modulator. A ICS-572B commercial board which is shown in figure 1 is adopted for the ADC/DAC and FPGA board. ICS-572B is a PMC module with 2-channel 105 MHz ADC, 2-channel 200 MHz DAC and with 4 million gate onboard Xilinx FPGA.

The board uses two 14-bit ADCs (Analog Devices AD6645) with a maximum sampling rate of 105 MHz. The sampling clock can be either internally or externally generated. The minimum ADC sample rate is 30 MHz. Both input channels are simultaneously sampled and transformer-coupled with turn rato of 4:1.

The outputs of the ADCs are connected to a Xilinx FPGA for direct processing of the ADC data. The ICS-572B includes a Xilinx Virtex-II FPGA (XC2V4000) that can be programmed by the user via a JTAG port or PCI communication.

On the output side, the ICS-572B uses two 14-bit high speed DACs (Analog Devices AD9857). The maximum simultaneous conversion rate is 200 MHz. The DAC has a built-in quadrature up-converter that allows the user to provide complex baseband input which is up-converted to a programmable IF (up to 100 MHz). For this purpose, the DAC includes the 32bit quadrature DDS. The DAC also provides a programmable clock multiplier.

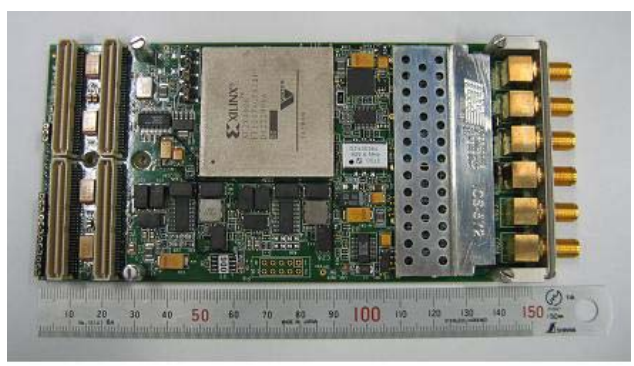

Figure 1: ICS-572B PMC Board.

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The communication between the ICS-572B board and host system is made using PCI bus. The QL5064 QuickPCI chip from QuickLogic is used for PCI interface solution. The performance of the QL5064 is 64 bit/66 MHz and automatically backwards compatible to 33 MHz or 32 bit

For the host system of the ICS-572B FPGA board, a Motorola VME processor module, MVME5100, is adopted. The main roles of the host system are the configuration of the FPGA board and the data acquisition.

The feedback logic based on the PI control is implemented in the FPGA by using VHDL. The I and Q component of the cavity field signal is fed into the FPGA using the ADC, which samples the RF signal four times during one period. The sampled I and Q components of the cavity signals are compared with the set value, which generates the error signal.

For a proportional control, the error signal is multiplied by the P gain. For an integral control, the error signal is multiplied by the I gain, and then integrated over time. The calculated proportional and integral control values are added then converted to an analogue signal by using DAC. The analogue signal from the DAC drives the IQ modulator. The set values and each gain value are written into the register in the FPGA by the host processor through a PCI communication. Therefore the set values and gains can be changed during the operation. The measured I and Q components of the RF signals are uploaded to the host board by using a PCI communication.

The development environment for the FPGA coding is as follows.

- coding language: VHDL
- synthesis tool: XST in ISE 7.1i from Xilinx
- implementation: ISE 7.1i from Xilinx
- mapping and routing: ISE 7.1i from Xilinx
- logic simulation: ModelSim SE 6.1b from Mentor

The flash ROM download file can also be generated in the ISE environment. The flash ROM files are downloaded by using a PCI communication.

The developed logic was verified by using a ModelSim simulation before implementing it into the FPGA. Errors in the code can be found through this simulation and this process also makes it possible to predict the FPGA behaviour and save on the development time [3].

PERFORMANCE TEST RESULTS

The schematic block diagram for the the overall LLRF control system is shown in figure 2. For the feedback test, we established the experimental setup by using a dummy cavity. As can be seen in figure 3, the PI control has shown a good performance in perturbation rejection. In addition, the feedback control with feed-forward could improve the transient response significantly. The shot-to-shot RF stability was measured and we found that the feedback control improved the shot-to-shot stability by an order of a magnitude compared with an open loop control.

For the high power RF test, the RF system was operated in pulse mode with 200 μs duration and 0.1 Hz.

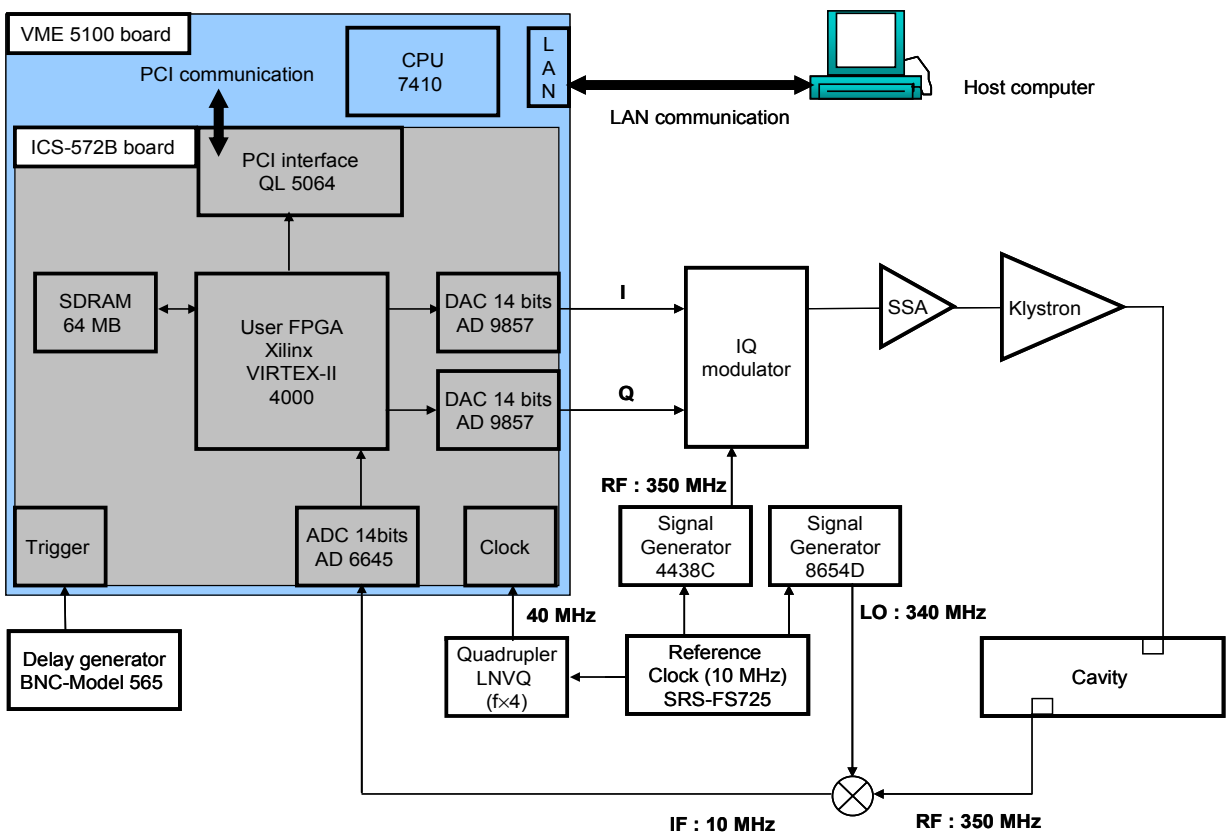

Figure 2: Schematic of the overall control system and experimental set-up.

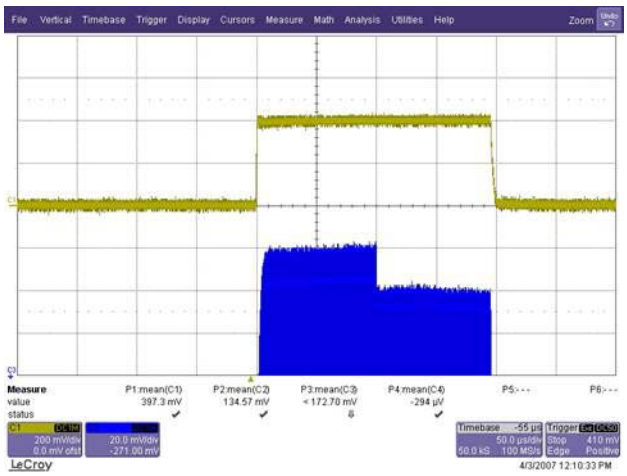

Figure 3(a): Cavity field response for Open-Loop Case. (upper: Forward RF power, lower: Cavity field).

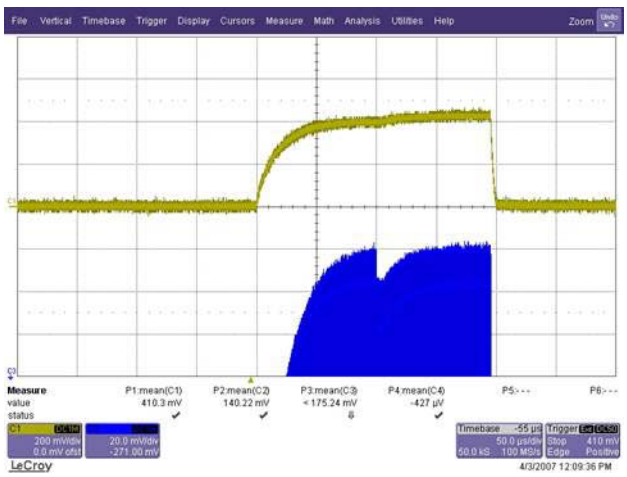

Figure 3(b): Cavity field response for feedback control. (upper: Forward RF power, lower: Cavity field).

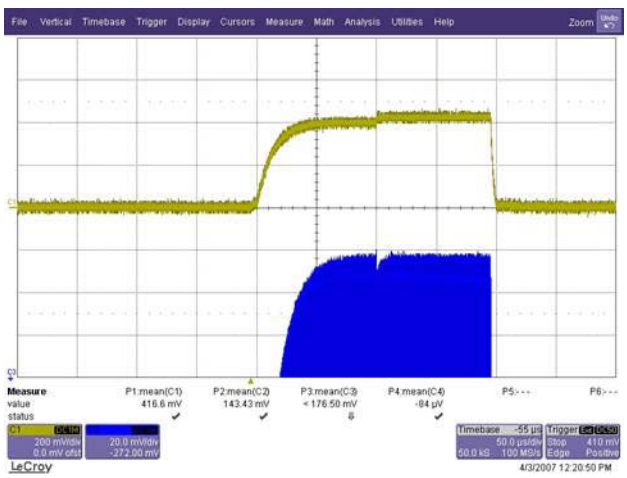

Figure 3(c): Feedback control with Feed-forward. (upper: Forward RF power, lower: Cavity field).

The measured RF amplitude variation and phase variation during a single RF pulse without beam were less than 0.2% and 0.3˚, respectively as shown in figure 4. The RF amplitude and phase of DTL cavity for 600 shots are shown in figure 5 and the results are summarized in Table 1. For 600 shots, the RF amplitude and phase were kept within ±0.7% and ±0.9˚ respectively, which meet the requirements of the RF control system.

In conclusion, the digital LLRF control system has been developed and tested. The test results showed that the control system meets the requirements. The performance with beam loading condition should be confirmed as future work.

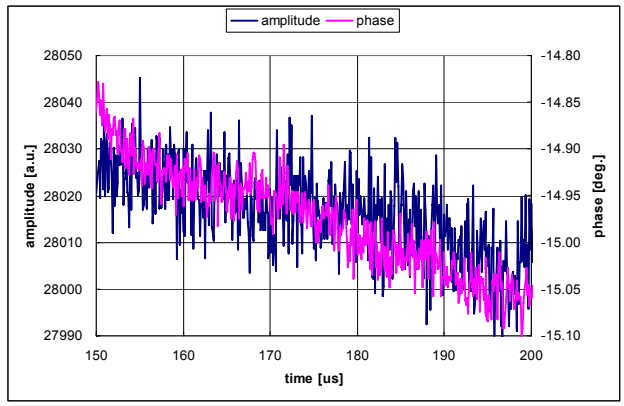

Figure 4: RF amplitude and phase in DTL cavity.

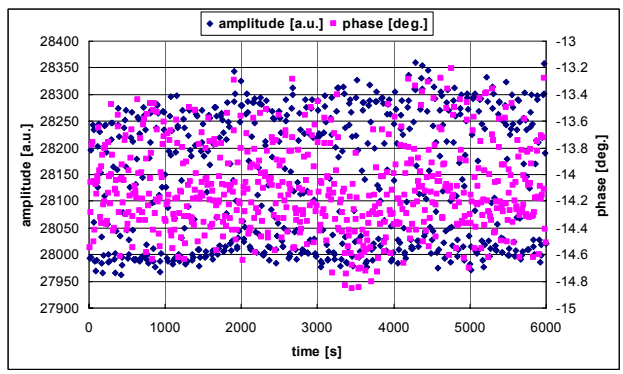

Figure 5: Pulse-to-pulse stability measurement results.

Table 1: Statistics for 600 shots measurements results

	amplitude	phase [deg.]
average	28139.1	-14.109
sigma	121.2	0.323
max error	0.79%	0.904
min error	-0.63%	-0.744

REFERENCES

[1] H. S. Kim, et al, “RF Characteristics of the PEFP DTL”, Proceedings of EPAC 2006, Edinburgh.

[2] M. E. Angoletta, “Digital Low Level RF”, Proceedings of EPAC 2006, Edinburgh.

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