ANALOG COMPONENTS CONFIGURATION AND TEST RESULTS FOR PEFP LLRF SYSTEM*

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Abstract

The PEFP LLRF system for the 3MeV RFQ and 20MeV DTL has been developed. The stability of ±1% in the amplitude and ±1˚ in the phase is required. Therefore, the drift of the analog components should be low to satisfy the requirement. Analog chassis as a prototype of LLRF system is configured and tested. RF components including an IQ modulator, an RF switch, a mixer, phase comparators, RF splitters, RF filters and trip circuit for high VSWR are installed in this chassis. This performs the shift of RF amplitude and phase from IQ signal, down-conversion to 10MHz IF signal, interlock for arc and high VSWR, and RF/clock distribution. The amplitude and phase stability of each component are measured to check the effect on the whole system performance. The detailed configuration and test results are presented.

INTRODUCTION

The 100 MeV proton accelerator is under development for the Proton Engineering Frontier Project [1]. For the first phase of the project, the 20 MeV accelerator which consists of the ion source, LEBT, RFQ and DTL has been developed and installed at KAERI site [2].

The LLRF control system for operating the 20MeV accelerator has been developed and tested , which consists of analog components and commercial digital control boards (ICS-572B FPGA board) [3]. Analog components are installed in the 19” rack chassis. The amplitude and phase stability of analog components are measured to check the effect on the performance of the LLRF control system.

ANALOG CHASSIS CONFIGURATION

Analog components were installed in the 19” rack chassis as shown in Figure 1, including an IQ modulator, an RF switch, a mixer, phase comparators, RF filters, power splitters, and circuits for VSWR trip. This performs error compensation for RF amplitude and phase due to IQ signal from the FPGA board, the down-conversion to 10MHz IF signal, interlock for HPRF system protection, RF and clock distribution, and phase measuring.

The shift of RF amplitude and phase was tested by adjusting IQ input signal of the IQ modulator (AD8345, Analog Devices, Inc.). The input and output frequency of IQ modulator is 350 MHz and IQ input signal is within ± DC 1V. In the feedback control, the full scale of DAC output for ICS-572B FPGA board is about 3.2 mA (0.32 Vpp, -6dBm) signal, so the matching circuit is required for the proper IQ signal between the DAC output of ICS-572B FPGA board and the input of IQ modulator, which consists of RF detector and OP amplifier.

An RF switch (ZASWA-2-500R, Mini-circuits) is used for the interlock of HPRF system protection. The RF switching time and isolation in RF off status were tested with a security box manufactured by TED (Thales Electron Devices). In the interlock test, the switching time of RF switch is within 10ns and the response time of the security box is about 2us. It is possible to cut off RF signal within about 3us in case of the interlock event. The isolation is below -80dB in RF off status. In the operation of 20MeV accelerator, interlock signal is circulator arc, RF window arc, klystron output window arc, and high VSWR. The circuit for VSWR trip consists of a divider IC and a switch. Figure 2 shows the VSWR trip signal measured in the HPRF test.

A 350MHz cavity's RF signal is down-converted to 10MHz IF signal in the analog chassis and transmitted to the FPGA board. A variable attenuator is used for matching signal level between down-converted 10MHz IF signal and ADC input.

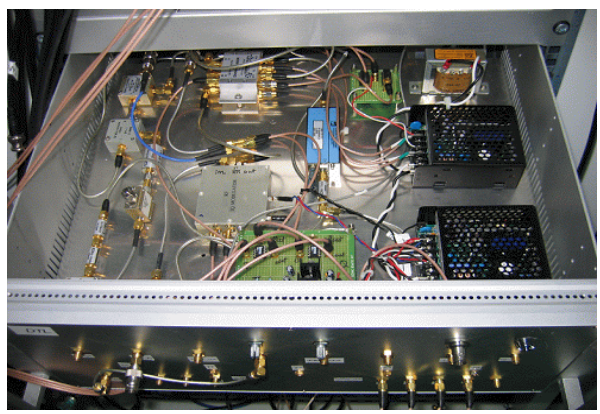

Figure 1: The installed analog chassis.

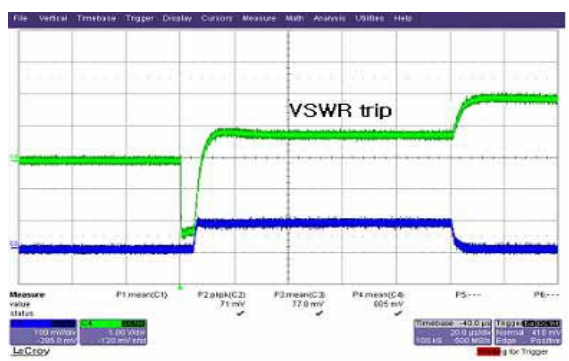

Figure 2: VSWR trip signal measured in the HPRF test.

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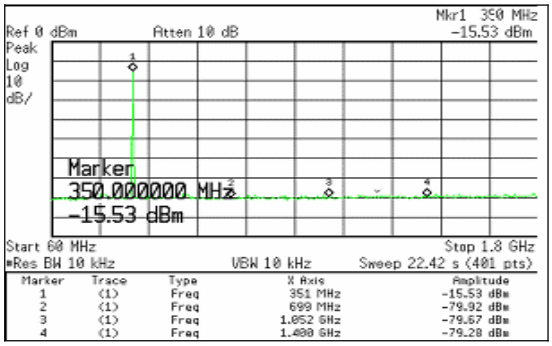

Figure 3: Output frequency response of analog chassis.

This analog chassis distributes 350MHz RF, 340MHz LO, 10MHz reference, and 40MHz clock. Also, this chassis includes the analog circuit for measuring the relative phase between DTL tanks, which consists of phase comparators, manual phase shifters, and divider IC.

The 350MHz output signal of analog chassis is transmitted to a drive amplifier to operate the klystron. 350MHz band pass filter is used for eliminating the harmonic and spurious signal of the IQ modulator as shown in Figure 3.

PHASE MEASUREMENT

Two commercial RF signal generators (one is 4438C for 350MHz RF and the other is 8648D for 340MHz LO, both from Agilent Technologies) are currently used for generating the 350MHz RF signal and the 340MHz LO signal in the RF test. The phase stability of RF signal generators is measured and the measured result is shown in Figure 4. The phase is stable enough for the 4438C RF signal generator but 8648D RF signal generator shows about 4 ripple. This means that 8648D signal generator is sensitive to temperature change of control room. This ripple of 340MHz LO signal causes the fluctuation of 10MHz IF signal and this brings the digital feedback control board to control incorrect cavity phase, although the cavity phase is not shifted in the feedback control.

In the feedback control for PEFP 20MeV accelerator, it is important that the relative phase between the RFQ and DTL should be maintained. In our case, LO signal lines is very short and the unstable LO signal have the effect on the RFQ and DTL equally. So, the relative phase between two cavities will be maintained. To check the relative phase, cavity pickup signal is used for reference signal in analog phase comparators and the relative phase between two cavities was measured by analog phase comparators and digital board simultaneously as shown in Figure 5. In this relative phase measurement, analog phase comparators measure the relative phase of 350MHz pickup signal and the digital feedback control board measures the relative phase of 10MHz IF signal affected by 340MHz LO signal. As shown in Figure 5, both the measured relative phase signals are maintained, and this means that the effect of the unstable LO signal disappeared.

DTL 4 tanks are operated by an RF source and the relative phase measurement between 4 tanks is required in the feedback control. The relative phase between DTL tanks was measured by analog circuit in analog chassis in the HPRF test as shown in Figure 6. The reference signal is the pickup signal of tank 2 and the measured fluctuation is caused by the fluctuation of the tank wall temperature.

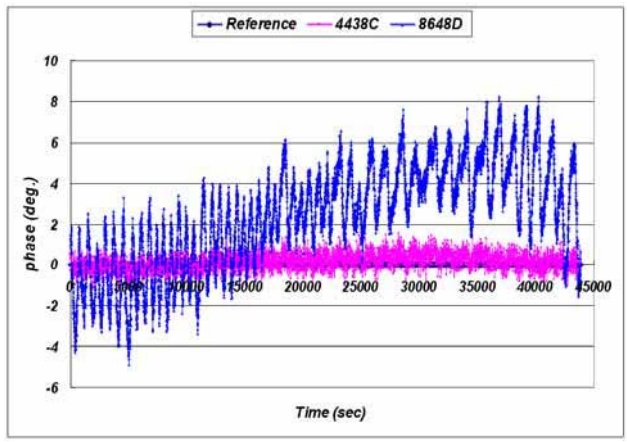

Figure 4: Phase stability of RF signal generators.

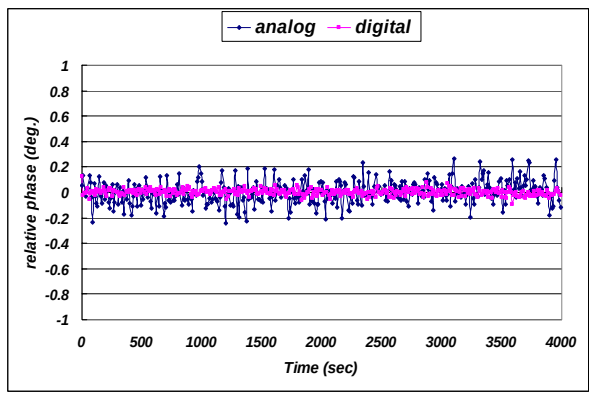

Figure 5: Relative phase measured between two cavities.

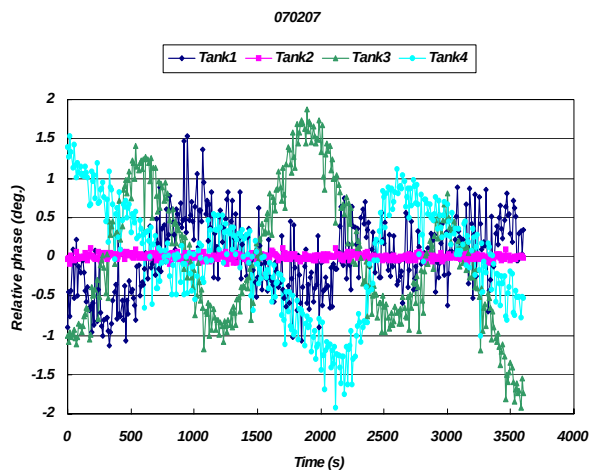

Figure 6: Relative phase measured in the HPRF test for the DTL.

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SUMMARY

Analog components were configured in the LLRF control system and this chassis has been operated for the RF and beam test. The amplitude and phase stability of analog components was measured. In the phase stability, the phase of 340MHz LO signal is unstable and sensitive to temperature change of control room. In the feedback control of 20MeV accelerator, it is important that the relative phase between two cavities should be maintained. In our case, the signal lines for 340MHz LO is very short and effects of the unstable LO signal are applied to the RFQ and DTL equally. We measured the relative phase between two cavities by using the analog circuit and digital feedback control board, and confirmed that the relative phase is maintained.

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