DESIGN OF THE MODULATOR FOR THE CTF3 TAIL CLIPPER KICKER

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Abstract

The goal of the present CLIC Test Facility (CTF3) is to demonstrate the technical feasibility of specific key issues in the CLIC scheme. The extracted beam from the combiner ring (CR), of 35 A in magnitude and 140 ns duration, is sent to the new CLic EXperimental area (CLEX) facility. A Tail Clipper (TC) is required, in the CR to CLEX transfer line, to allow the duration of the extracted beam pulse to be adjusted. It is proposed to use a stripline kicker for the tail clipper, with each of the deflector plates driven to equal but opposite potential. The tail clipper kick must have a fast rise-time, of not more than 5 ns, in order to minimize uncontrolled beam loss. Several different options are being investigated to meet the demanding specifications for the modulator of the tail clipper. This paper discusses options considered for the fast, high voltage, semiconductor switches and shows results of initial tests on the switches.

INTRODUCTION

The aim of CTF3 is to investigate the feasibility of a high-luminosity, multi-TeV, linear e^+ e^- collider. The latest CLIC Test Facility (CTF3) is currently being built and commissioned at CERN, the European Laboratory for Particle Physics, by an international collaboration.

The CTF3 facility [1] will, by 2009, include a 70 m long linac followed by a 42 m delay loop, an 84 m combiner ring (CR) and a CLic EXperimental area (CLEX). The beam pulse extracted from the CR is 35 A and 140 ns: a kicker, termed a "Tail Clipper" (TC), is required in the transfer line to CLEX to adjust the length of the beam pulse. The tail-clipper must have a fast rise-time, of 5 ns or less, to minimize uncontrolled beam loss. The maximum required duration of the tail clipper field is 140 ns: the flatness of the kick pulse is not important as deflected beam is to be thrown away. It is proposed to use a stripline kicker for the tail clipper, with each of the deflector plates driven by an equal but opposite polarity pulse. The product of the potential difference between the striplines and the overall stripline length is 4.8 kV·m. Table 1 shows the tail-clipper kicker system parameters.

Table 1: Tail-clipper kicker system parameters

Beam energy	200	MeV
Total kick deflection angle	1.2	mrad
Stripline plate separation	40	mm
Field rise-time (0.25% to 99.75%)	≤5	ns
Pulse duration	up to 140	ns
Initial repetition rate	5	Hz
Nominal repetition rate	50	Hz
Timing jitter	≤1	ns
Pulse voltage per plate · plate length	±2.4	kV·m

On leave from KEK, Japan.

DESIGN CONSIDERATIONS

General

The angle of deflection (θ_E), in radians, due to an electric field between stripline plates, is given by:

$$\theta_E = \arctan\left(\frac{V \cdot l_s \cdot c}{d \cdot p \cdot \beta \cdot c}\right) \quad (1)$$

where V is the potential difference between the deflector plates, l_s is the overall length of the deflector plates, d is the plate separation, $\beta \cdot c$ is particle velocity, c is the velocity of light in free space ($3\text{x}10^8$ m/s), and p is the beam momentum in units of GeV/c.

The angle of deflection (θ_B), in radians, due to a magnetic field is given by:

$$\theta_B = 0.3 \cdot B \cdot l_s / p \quad (2)$$

where B is magnetic flux-density [T].

It can be shown that the deflection due to the magnetic field is independent of the impedance of the striplines and these deflections are equal for $\beta=1$. In order to make use of commercially available components, such as coaxial cable and feed-throughs, it is preferable to select a system impedance of 50 Ω. A carefully matched high bandwidth system is needed to fulfil the fast rise-time requirement. Each system is therefore composed of a 50 Ω Pulse Forming Network (PFN), a fast switch, 50 Ω stripline plates and a matched terminating resistor. Fig. 1 gives the basic circuit diagram of the tail clipper system.

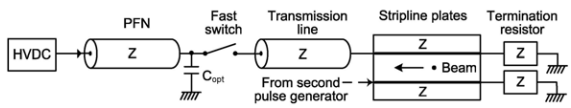

Figure 1: Schematic circuit of kicker system.

Striplines

In order that the electric and magnetic fields seen by the beam do not annul each other the striplines must be "charged" from the CLEX (beam exit) end (Fig. 1). A 1.2 mrad deflection requires ±2.4 kV·m for the stripline deflector plates. To establish the requisite deflection fields the applied pulse wave-front must fully propagate along the stripline. For striplines, with no magnetic or dielectric material, of overall length l_s, subdivided into N sections and a relativistic beam bunch spacing of l_b, it can be shown that the permissible pulse rise-time (t_p) is:

$$t_p = \left(l_b / c\right) - \left(2 \cdot l_s / (N \cdot c)\right) \quad (3)$$

Fig. 2 shows a plot of the required magnitude of pulse voltage, per stripline, versus total stripline plate length. In order to make use of commercially available 50 Ω feed-throughs the pulse voltage should be below 5 kV; thus a

minimum overall stripline plate length of 0.5 m is required. The acceptable CTF3 field rise-time (l_b/c) is 5 ns which would limit the pulse rise-time to less than 1.67 ns, for a 0.5 m stripline. To mitigate this effect the stripline can be mechanically sub-divided into N sections of equal length (see Eq. 3) with each section energized a time delay ($l_s/(N{\cdot}c)$) after the previous section, starting with the section at the beam entrance.

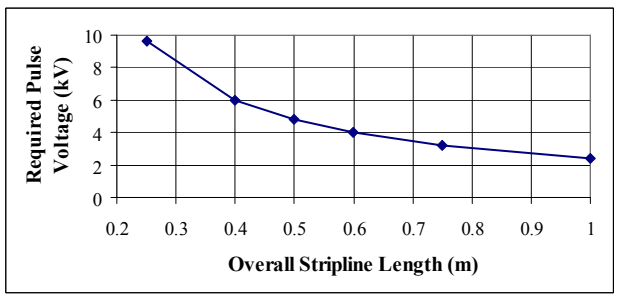

Figure 2: Required pulse voltage, per stripline plate, versus overall stripline length for 1.2 mrad deflection.

Fig. 3 shows a plot of permissible rise-time of the input pulse for overall stripline plate lengths of 1 m, 0.75 m and 0.5 m subdivided into between 1 and 5 sections.

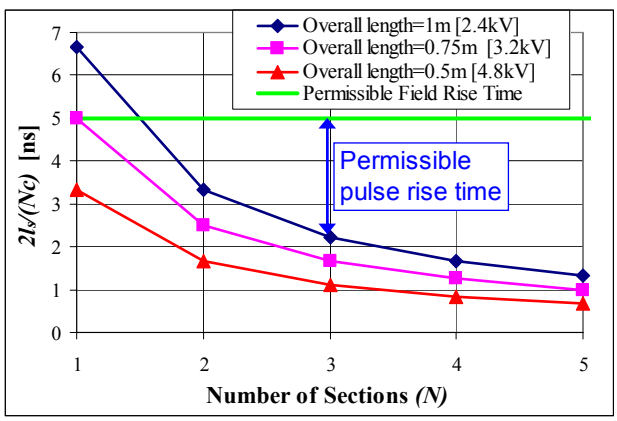

Figure 3: Permissible rise-time of input pulse versus number of stripline sections for overall stripline lengths of 1 m, 0.75 m and 0.5 m.

Switch

To satisfy the specification for jitter of ≤1 ns a semiconductor switch is required. Several types of semiconductors have been considered for the TC:

- MOSFETs;
- Fast Ionization Dynistor (FID) [2];
- Behlke MOSFET based switch [3].

Stacked MOSFET Switches (SMS) have been developed at TRIUMF: these systems have voltage ratings up to 12.5 kV and have been tested at burst-rates of up to 3 MHz [4]. The latest design uses a MOSFET with a rating of 1 kV DC and 72 A pulse; the fall-time of the FET voltage has been measured to be <3 ns [5]. Recent measurements on an SMS gave 10% to 90% rise-time of 3.7 ns for a 4.8 kV pulse [6]. A version with less series FETs, to generate lower voltage pulses, would be expected to give a faster pulse rise-time.

It is planned to evaluate a FID device, the FPG 5-01M122S144N, which has a specified output voltage of 5 kV into 50 Ω with a rise-time of 1.5 ns to 2 ns.

Behlke, high voltage, MOSFET switches are available with suitable datasheet rise-times. One of these switches has so far been tested (see below).

SIMULATIONS

To gain a good understanding of the circuit parameters that significantly affect the rise-time of the load-current the schematic shown in Fig. 1 has been simulated using PSpice. The nominal parasitic inductance of the switch is approximately 50 nH: with a 50 Ω PFN and 20 pF drain capacitance the transit time of the switch was chosen to give a 10% to 90% load current rise-time of 1.7 ns. Parameters varied include: switch drain capacitance; switch parasitic inductance (Lswitch); PFN impedance (Zpfn) and load impedance (Zload). The curves of 10% to 90% rise-time of load current, shown in Fig. 4, are, in general, relatively flat for drain capacitance values of 100 pF and above. With 100 pF of drain capacitance:

- 50 nH of switch inductance increases the rise-time by 0.38 ns (33%) relative to no switch inductance;
- A PFN impedance of 25 Ω, instead of 50 Ω, increases rise-time from 1.53 ns to 1.91 ns (25%). Replacing the PFN by a capacitor (e.g. of 8 nF) increases the rise-time to 2.76 ns – but would allow a lower drain voltage.
- The load impedance has little effect upon rise-time.

Therefore, to minimize rise-time, the parasitic inductance of the switch must be minimized and the PFN should be a relatively high impedance coaxial cable.

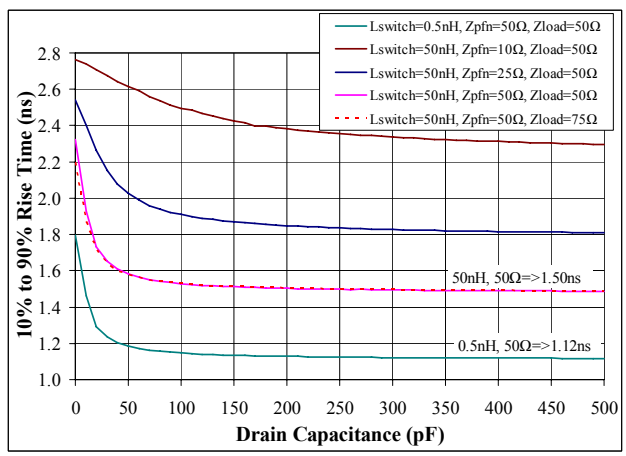

Figure 4: Predicted rise-time of load current for various values of switch inductance, PFN impedance, load impedance and drain capacitance.

MEASUREMENTS

A Behlke HTS-50-08-UF switch [2], mounted on a low inductance circuit board, has been tested. The PFN, connected to switch drain, was charged using an HV power supply with an adjustable output of up to +3.5 kV. A 50 Ω coaxial cable interconnected the switch cathode and the low inductance, 50 Ω, resistive load. A Bergoz

Current Transformer (CT), the CT-D1.0-B, which has a specified rise-time *(t_{CT})* of 0.7 ns, together with a Tektronix TDS5054B oscilloscope, were used to measure load current. The specified bandwidth of the oscilloscope, 500 MHz, corresponds to a 10% to 90% rise-time *(t_{OSC})* of 0.7 ns [6, 7].

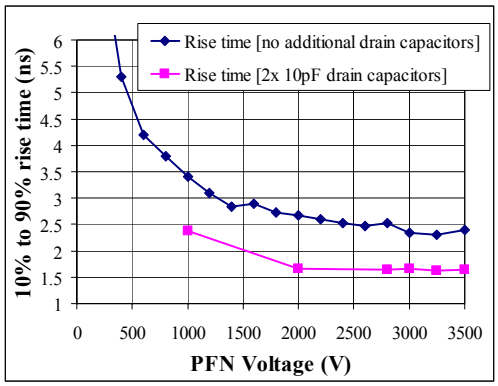

Figure 5: Measured 10% to 90% rise-time of load current, versus PFN voltage, with and without 20 pF capacitance.

The estimated inductance of the Behlke switch, together with connections to the PFN and transmission cable, is 50 nH. The layout allows for two low inductance capacitors to be mounted between switch drain and ground (C_{opt} in Fig. 1). Two capacitors, each of 10 pF, are mounted for several measurements. Fig. 5 shows measured 10% to 90% rise-time of load current, as a function of PFN voltage, with and without 20 pF of drain capacitance. The rise-time reduces as PFN voltage is increased to ~2 kV, but then remains relatively constant.

Fig. 6 shows the measured load current, for 3 kV PFN voltage, with 20 pF of drain capacitance. The top of the current droops due to losses in the PFN coaxial cable, which is acceptable for the TC since the deflected beam is to be discarded. The maximum of the flat-top load current is ~33 A, indicating an on-state resistance of ~4.5 Ω for the Behlke switch, corresponding to a voltage pulse of 1.65 kV. A voltage pulse of ±2.4 kV is required for 1 m plates so that the PFN voltage must be at least 5.1 kV. The oscillations at the front end of the flattop are due to a high frequency impedance mismatch of the load.

The measured rise-time *(t_{MEAS})* of the load current, at 3.5 kV PFN and with 20pF of drain capacitance, is 1.7 ns (Fig. 5). Assuming that neither the CT nor oscilloscope cause overshoot of the measured pulse, the actual rise-time of the current *(t_{CUR})* can be estimated, using Eq. (4) [8], to be 1.4 ns, i.e. ~23% error relative to the 1.7 ns measured.

$$t_{CUR} = \sqrt{(t_{MEAS})^2 - (t_{CT})^2 - (t_{OSC})^2} \qquad (4)$$

A higher bandwidth measurement system is required to determine the actual rise-time of load current. Based on Eq. 4, and assuming a load current rise-time of 1.4 ns, an oscilloscope and CT each with a bandwidth of 1 GHz would result in a measured 10% to 90% rise-time error of 6.2%. To obtain ~6% error for a rise-time of 1.4 ns 1% to 99% (0.25% to 99.75%) requires a bandwidth of 2 GHz (3 GHz) for both the oscilloscope and CT.

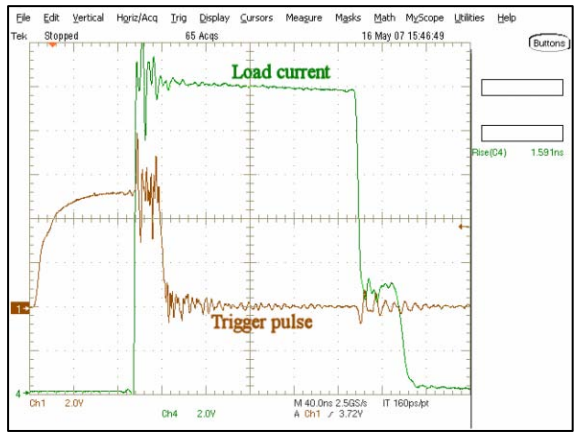

Figure 6: Measured load current, for 3 kV PFN voltage, with 20 pF of drain capacitance (40 ns/div).

The measured 1.7 ns rise-time, 10% to 90%, was subsequently reduced to 1.6 ns (Fig. 6) by replacing: (a) the 2 m coaxial cable between switch and load by a 0.6 m length, and (b) a 10 ns C-50-2-1 FRNC cable between CT and scope by a 3 ns long RG58 coaxial cable.

CONCLUSIONS

A deflection of 1.2 mrad, for the 200 MeV beam, can be achieved with ±2.4 kV pulses and an overall stripline plate length of 1 m. However, to achieve a kick rise-time of <5 ns, a segmented stripline kicker is required: 3 sections, each of 0.33 m, allow a voltage pulse rise-time of 2.75 ns. A HTS-50-08-UF Behlke switch, in a low inductance configuration, with a 50 Ω PFN and 20 pF drain capacitance, has been tested to 3.5 kV PFN and a current rise-time (10% to 90%) of 1.6 ns measured. However, with a 50 Ω PFN and load, a PFN voltage of at least 4.8 kV is required: it is planned to test other HV, fast, semiconductor switches.

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