

DIGITAL MASTER OSCILLATOR RESULTS FOR THE ISIS SYNCHROTRON

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Abstract

Rutherford Appleton Laboratory in Oxfordshire is home to an 800MeV synchrotron particle accelerator called ISIS. Its main function is to direct a beam of protons into a heavy metal target to produce neutrons for scientists to analyse condensed matter. A second harmonic system is being developed to upgrade the beam current from 200 μ A to 300 μ A in order to drive a second target station. This is being achieved by the inclusion of four second harmonic cavities to increase the width of the RF bucket. In the past the six fundamental cavities were driven by an analogue Master Oscillator but the extra cavities will bring more difficulty in the phasing of the system. This could be more easily and precisely controlled by using a Direct Digital Synthesis system (DDS) as the heart of a new digital Master Oscillator.

This paper describes the results of the setting up and performance of the prototype instrument so far and the implications it has for the synchrotron.

INTRODUCTION

The Fundamental system is relatively easy to phase as the cavities are arranged in geometrically opposing pairs in the ring and so only require three pairs of drive signals. With the introduction of four 2nd Harmonic cavities (2RF) in close proximity in superperiods 4, 5, 6 and 8, the phasing becomes extremely complex. A phase θ has to be introduced which is a dynamic phase shift between the Fundamental and the 2RF cavities, along with the static phase between each 2RF cavity due to their position in the ring.

The first prototype PCB has been designed and tests have been carried out to see if all ten cavity drives can be controlled by this one board using digital techniques.

CIRCUIT DESIGN

Concept

The system was initially put together using evaluation boards for the analogue to digital and digital to analogue converters (ADC & DAC) and the Field Programmable Gate Array (FPGA) device. The core of the synthesised waveform generation was then based around a DDS system coded in the FPGA as described in the previous paper [1]. The system simply uses a digital step value to set the frequency required and a digital offset value to set the phase shift.

Analogue

The requirement of the system is: 1V \equiv 500kHz, so using a 2²¹ counter with a 132MHz system clock, the step value for 500kHz is: $(500k * 2^{21})/132M \equiv 7944$ steps. The on board ADC used was a 16-bit 10MSPS ADS1605 with an input range of -4.4V to +4.4V. So 1V equates to $(65536/8.8V) \equiv 7447$ steps. A gain of $(7944/7447) = 1.06674$ is therefore required to correct the step value. The formula is:

$$V_o = \text{diff } V_{in} - (4.4V - (0.06674 * \text{diff } V_{in})).$$

This adjustment was achieved using low offset Op Amps (LT1097s), a very stable 1ppm/ $^{\circ}$ C precision voltage reference and 10ppm resistors.

Digital

The heart of the circuit contains a Lattice FPGA ball grid array chip [2]. The code utilises the on-chip Phase Locked Loop (PLL) to multiply the crystal oscillator frequency, Look Up Tables (LUTs) for the DDS systems and gates for all the system control logic.

The binary outputs from the ADC and the θ Phase input port are connected to the FPGA along with the front panel digital potentiometers, 'Machine Start' and the synchrotron's 'Delta-P' timing signals.

The FPGA outputs are connected to thirteen DACs which drive the ten cavity channels, two reference channels and one spare channel. The reference channels are required during setup to measure the relative phase shift between the output channels for the Fundamental and 2RF cavities. Outputs are provided to drive the front panel displays in order to run tests and set up parameters along with spare outputs for future development.

The FPGA programming was performed using a JTAG port and an onboard flash memory device which allowed the chip (and memory) to be programmed directly. The FPGA was then re-programmed from the memory on the next power up. Programmable test points were included on the board along with 16kbytes of onboard EEPROM available for parameter storage.

The reference frequency of 33MHz is from an Oven Controlled Crystal Oscillator (OCXO) and is stable to 10ppb with a calibration frequency of 0.1ppm. This was multiplied by four using an onboard PLL to give a system clock of 132MHz. The whole system is therefore tied to the stability of this crystal.

The OCXO requires 72 hours initial running to stabilise and will be constant thereafter but a battery backed system was designed into the board to keep the OCXO running in the event of a power down to optimise the oscillator's stability.

PCB TECHNIQUES

Ground planes

Due to the FPGA being a 672 ball grid array device, the PCB became a ten layer board in order to facilitate tracking to all connections.

The top layer contains all the tracks for the DAC's fast input and enable signals. The layer directly below is the ground plane. All the power connections to the various analogue and digital parts were separated accordingly as split power planes.

Grounded mount holes were set around the perimeter of the PCB and two more centrally to connect a chassis earth to the board as seen in Figure 1.

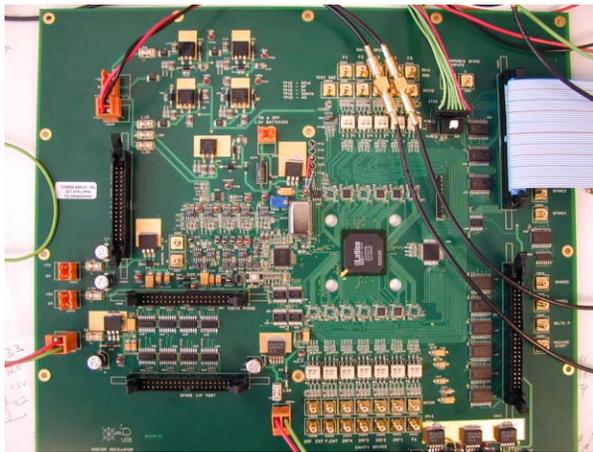


Figure 1: Master Oscillator PCB.

General

All decoupling capacitors for the FPGA were fitted on the bottom layer directly beneath the chip using 0402 SMT devices.

The enable signals to all DACs were from an ICS8532 16-output PECL driver connected with equal distance serpentine tracks to ensure all the DACs switch on at the same time.

SOFTWARE DESIGN

The software was written in VHDL and was constructed by writing 'components' for the various operations the main code required. For example a component was written to create an I2C driver to handle the serial data to and from the onboard EEPROM. This was then tested discretely using ModelSim. The component could then be instantiated in the main code.

Most of the code was constructed using state machines which proved to be the best way to manage and debug the programs.

The LUTs were constructed by using the IP manager in the Lattice Lever software environment [3]. The sinewave tables were constructed using Excel and pasted into a text file so the IP manager module could read the file and construct the sine LUTs thus making the process

easier. The PLL was also constructed using the IP manager.

The digital potentiometers and de-bounce codes were developed separately and were constructed around 21 bit counters in order to match up with the phase accumulators in the DDS systems.

The data handling proved to be the hardest part as this was achieved by tri-stating lines to set the data direction to and from the system running in normal mode or test mode or interfacing to and from the EEPROM. It also had to allow access to download parameters to and from another Master Oscillator (spare).

RESULTS

Testing

After allowing the OCXO to run for 72 hours to stabilise, it was checked against a satellite receiver frequency standard. This showed the frequency to be accurate to within 1Hz with no significant drift observed over a week.

The board was programmed with test code and sine waves were observed showing that all connections to the FPGA were ok. The code was then developed to produce waveforms through the other channels.

The next development was to include in the code the digital potentiometer components so the frequency and phase shift could be tested. The integral push button in the potentiometers were de-bounced and utilised to toggle between a coarse and fine setting when adjusting the frequency and phase shifts. Two channels were then tested by creating a waveform at one frequency and another at twice the frequency as shown in Figure 2. The frequency and phase shift was successfully adjusted using the potentiometers along with the coarse and fine facility.

The θ phase and frequency law input tests have still to be done but as the core of the system has been shown to work correctly it shouldn't be a problem.

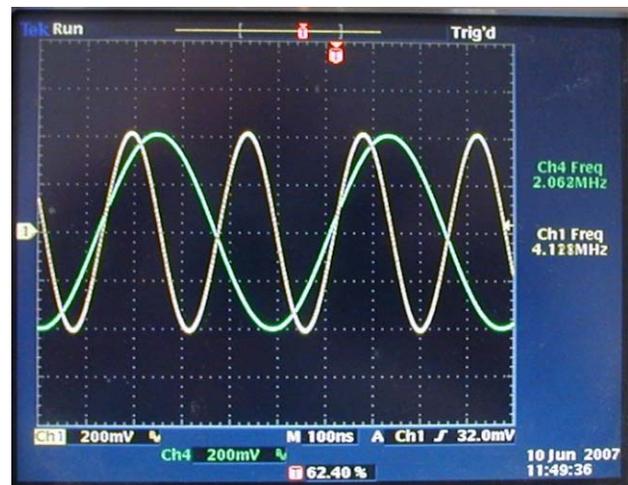


Figure 2: Two output channels showing a phase shifted 2RF signal and a fundamental waveform.

Next step

The chassis incorporating integral power supplies and front panel displays has still to be built and once two units have been completed then the data storage and communications can be tested fully before the unit can be commissioned in the synchrotron itself. This will be the subject of a future paper.

SYSTEM SPECIFICATIONS

• System clock rate	132MHz
• Crystal frequency	33MHz
• Crystal stability	10ppb
• Crystal frequency calibration	0.1ppm
• Frequency change time	<10ns (one fclk)
• Phase shift resolution	172 μ degrees
• Frequency resolution	63Hz
• Simulated sine wave table	2MB
• Frequency range	1.3MHz to 6.2MHz
• Output channels	13
• FPGA (Lattice LFCEP20)	1.5M gates [2]
• ADC (TI ADS1605)	5MSPS 16 bit
• DAC (AD AD9748)	165MSPS 8 bit
• On board data storage	16kbytes
• On board flash memory	8M bit
• OCXO battery backup	2 days
• Digital potentiometers	4.
• Display drives	9 x 7 segment led
• Programmable test pins	10.
• Spare test outputs	6.
• Spare test inputs	32.

CONCLUSIONS

The project has progressed from the evaluation boards to one custom designed PCB. The readings from the oscilloscope have shown that digitally generated sine waves can be cleanly produced from the FPGA, and that the frequency and phase shifts can be accurately set up using digital potentiometers.

Development is ongoing at the moment and code is being developed to allow parameters to be setup dynamically and stored when commissioning is to be performed. For example, by use of front panel digital potentiometers and displays, a test can be selected to adjust the static offsets between the cavities while the machine is running and store the results using I2C serial communication between the FPGA and the onboard EEPROM. These values would then be available again on power up if a power down situation has occurred.

Parameter data can also be loaded to a duplicate unit and, because it is digitally stored, would produce a perfect spare. Any difference would be down to the performance of the OCXO which has proved to be extremely accurate.

Future tests can be added by developing and simulating code and using the spare input facilities therefore reducing the need to add further hardware.

The PCB will also be used as a development board to utilise the FPGA's onboard Digital Signal Processing (DSP) blocks. At the moment the output filtering is being done simply by using roll-off capacitors, but if the on chip DSPs can be successfully utilised then precise digital Finite Impulse Response low pass filters can be constructed and implemented in the system. This will also be discussed in a future paper.

Implications arising

- The Fundamental and 2RF cavities are driven directly therefore removing the need for analogue phase splitters.
- If connected to the machine's Delta-P and Machine Start signal and the RF loop signals digitised, the RF law can be stored in the FPGA thus eliminating the summing amplifier and Frequency Law Generator.
- The stability of the OCXO could be utilised to provide the Delta-P and the Machine Start signals as well as other timing pulses for the synchrotron.
- The analogue drives that determine the phase relationship between the Fundamental and 2RF cavities could be replaced with digital units so being able to connect directly with the FPGA rather than through ADCs.
- The FPGA's built in DSP blocks could be utilised to produce the filters for the output drives and also provide filtering for beam compensation.
- The present code and sinewave tables utilises approximately a quarter of the FPGA's capacity so providing available space for future expansion for more system controls.
- The volume of the hardware presently required to control the synchrotron can be drastically reduced with this digital system. This would in turn reduce noise and improve servicing.

ACKNOWLEDGEMENTS

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Also acknowledgement is due to Mike Glover for his initial suggestion to use DDS systems to utilise the ease and accuracy of digital techniques to solve the phasing problems that occur in a synchrotron upgrade of this sort.

REFERENCES

- [1] C. Appelbee *et al*, "Digital Master Oscillator for the ISIS Synchrotron", EPAC'06, Edinburgh, 2006.
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