POWER MODUALTORS FOR FERMI'S LINAC KLYSTRONS

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Abstract

The conventional line type modulators now in use for ELETTRA will have to be replaced for FERMI due to the increase in the pulse repetition frequency (PRF) from 10 to 50 Hz [1]. The requirements for the FERMI modulator are as follows. The klystron which will be used is a Thales TH2132 with a microperviance of 1.9-2.1 uA/V$^{3/2}$. The peak voltage from the modulator is 320 kV, and the current is 350 A. The pulse width is 4.5 us, with a PRF of 50 Hz. Flat top should be better than ±0.5 % of the peak voltage and pulse to pulse ripple better than ±0.1 % of the peak voltage. Prototypes for an upgraded line type modulator and a solid state induction type modulator [2] are in fabrication. The solid state design uses eight induction cells, each cell driven by two parallel Insulated Gate Bipolar Transistors (IGBT). Each IGBT will power an amorphous core with up to 4.16 kV and 1.925 kA for up to 5 us. A single turn is passed through the aperture of each of the cells, inductively adding the pulse voltages. The output from the modulator is then fed to a conventional pulse transformer to reach the 320 kV requirement. This paper presents the system design of both modulator types. Details of the IGBT drivers, control electronics, IGBT and klystron protection and the charging supply for the solid state modulator are also presented.

FERMI MODULATOR REQUIREMENTS

The requirements for the klystron modulators for FERMI are given in Table 1. Prototypes of a conventional line type modulator (PFN) and a solid state modulator (SSM) are currently in the procurement and fabrication stage. The scope of the program is to have dedicated test stands for comparing the two technologies in terms of performance and reliability. The SSM will be a hybrid design using a conventional pulse transformer in order to avoid an R&D program that would be required for a multi-turn inductive adder topology. Prototypes of both the PFN and the SSM will be ready for testing by the end of 2007, and the decision on which technology to use for the production modulators will be made in the first quarter of 2008. Production of the 14 FERMI modulators will begin in 2008.

Table 1: FERMI modulator requirements

Peak Voltage	320 kV
Peak Current	350 A
Pulse Width	4.5 µs
PRF	50 Hz
Rise/Fall Time	<0.5 µs
Flat Top	±0.5 % V_{peak}
Pulse Ripple	±0.1 % V_{peak}
Number of Modulators	14 + 1 spare

CONVENTIONAL MODULATOR DESIGN

The PFN modulator is a line type design that uses an e2V CX1536X thyratron as the switch, and is essentially an upgrade of the existing ELETTRA modulators, modified to operate at 50 Hz [3]. Several modifications will be made to the existing design. The high voltage power supply will be a 30 KV high stability capacitor charging unit, able to guarantee a pulse to pulse repeatability better than 1x10^{-4} with no need for a de-q'ing circuit. The new pulse forming network, will give a 4.5µs pulse length, with a nominal ripple of ±0.5%. The first unit has been already tested at ELETTRA showing less than 0.5% pk-pk voltage ripple. It will be water cooled in order to withstand the 50Hz operation. We plan to use a new pulse transformer with increased power handling and voltage droop of less than 1 % which will be compensated by a 1 % rise from the pulse forming network. Finally there will be new interlock and control systems, as these were the major cause for downtime with the ELETTRA modulators.

All of the major components to build the conventional modulator are now in house, and fabrication will begin this summer.

SOLID STATE MODUALTOR DESIGN

The SSM design uses two 6.5 kV, 800 A IGBTs to drive each of the primaries of eight magnetic cores. The cores are stacked in a column with a single secondary turn passing through the apertures, inductively adding the primary voltages. The output of the inductive adder is then stepped up by a conventional pulse transformer which is connected to the cathode of the klystron. A schematic of the system is shown in Figure 1.

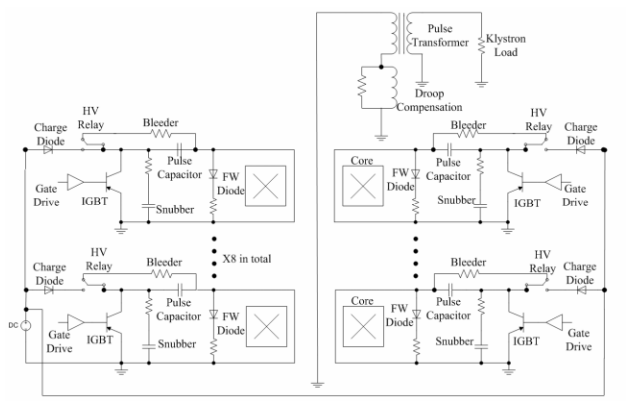

Figure 1: Schematic of solid state modulator.

The specifications for the SSM are given in Table 2. Figure 2 shows an exploded view of one core case assembly, while Figure 3 shows the erected stack of cores

with the IGBT drive boards, freewheeling diodes and structural supports.

Table 2. Specifications for the solid state modulator

Number of Cells	8
Number of IGBTs/Cell	2
Transformer Ratio	11:1
Nominal IGBT Voltage	3636 V
Fault IGBT Voltage	4156 V
IGBT Current	1925 A
Core Dimensions	135×430×25.4 mm
# of Cores/Cell	3

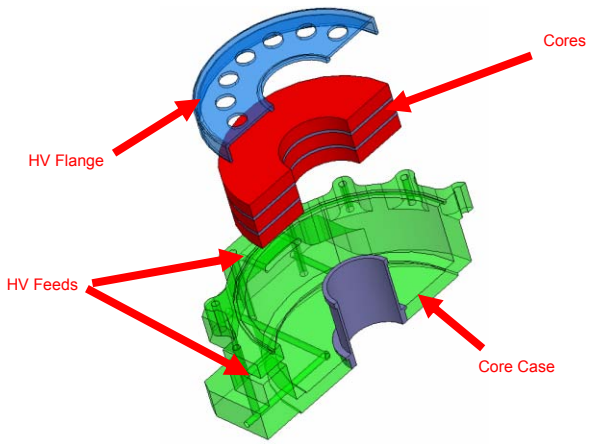

Figure 2: Core case assembly.

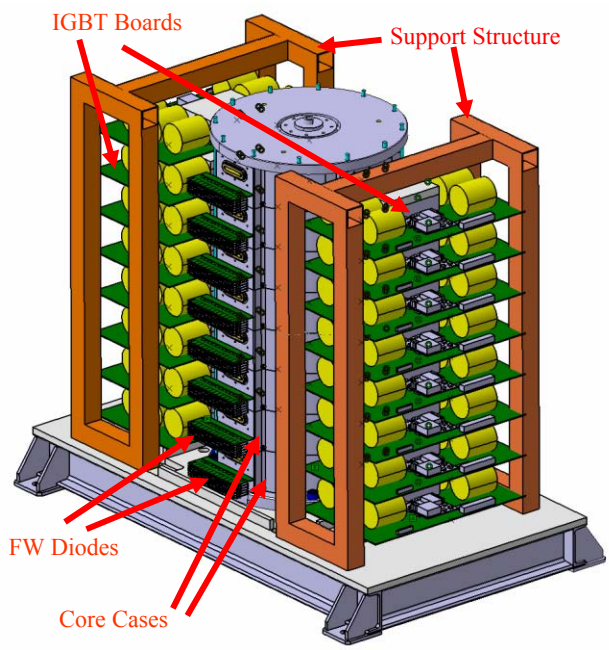

Figure 3: Assembled solid state modulator.

Each cell is made from three amorphous cores of 425 mm OD by 135 mm ID and one inch thick. The cores are enclosed in an aluminium housing that is water cooled and filled with oil. Each core case has three high voltage feedthroughs, one for each of the IGBT boards, and one for the freewheeling diode. An aluminium pipe through the center of the core stack forms the secondary. A DC current is run on the secondary to reset cores, as well as the pulse transformer.

The IGBT boards are composed of an IGBT and a driver, an array of six 14.7 µF, 4500 V metalized film capacitors, a charging diode and a high voltage vacuum relay to isolate each of the boards. A snubber circuit is used to protect the IGBTs from switching transients, and a current viewing resistor and high voltage divider are used to view the emitter current and the collector to emitter voltage. These signals are analysed on a daughter board which can quickly remove the gate drive in the event of a load fault. The gate drive circuit is based on a design from SLAC [4]. The freewheeling diodes are made from an array of twelve parallel by six series APT15DQ120BCT, 1200 V, 15 A diodes with both current and voltage sharing networks.

A block diagram of the electronics for one cell is shown in Figure 4. The operation of the system is as follows. The discriminator board will truncate the input pulse in the event of a pulse width fault, and not allow pulses at greater than 50 Hz. The pulse is then ANDed with various other fault signals such as loss of the core reset or a driver fault, and fanned out to a trigger board for each of the 16 IGBTs. The trigger boards provide a trigger signal for each of the IGBT drivers as well as report IGBT and driver faults. The triggers for each IGBT can be independently delayed by supplying a digital word to a digital delay line chip. These delays are useful in shaping the klystron pulse and in avoiding ringing caused by the leakage inductance of the transformers and the stray capacitance [5].

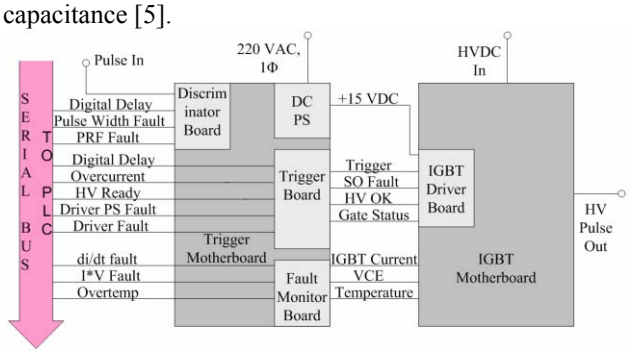

Figure 4. Block diagram of cell electronics.

The current will be monitored for each IGBT with a current viewing resistor on each of the power emitter leads, and the voltage will be monitored with a pulse compensated resistive divider. A fault board will monitor these signals, as well as the IGBT's heat sinks temperature. A fault will be detected in the event that both current and voltage are above a certain threshold, or if either a current limit or an IGBT temperature limit are exceeded. In each event the gate drive for that particular IGBT will quickly be removed, commutating the IGBT. Other faults which will also commutate the IGBT are an SO fault detected by the Concept IDG515E gate drive circuit and a HV OK fault from the drive board. For each of these faults, a high voltage relay will open, disconnecting the IGBTs for that cell, and the high voltage power supply will be re-programmed to run at a

higher voltage to compensate for the lost cell until maintenance can be performed. These faults, as well as other information such as the digital delays will be communicated by a serial link to a programmable logic controller (PLC).

Each modulator will have a dedicated PLC for the control system. The PLC will also be used for control of and monitoring of the klystron and waveguide vacuum and water systems, the klystron solenoid supply, and communication with the low level RF system. The PLC in turn communicates with the FERMI control system via Ethernet.

The klystron pulse will have to be compensated in order to reach the flat top requirements because of capacitance droop and droop associated with the magnetizing inductance of the cores. An R-L circuit was selected for droop compensation because it needs no active components and the power dissipated by the network is tolerable in this application. The results of a SPICE simulation showing the uncompensated and compensated klystron pulses is shown in Figure 5. The network used in this simulation is an inductance of 2 μH and a resistance of 300 mΩ.

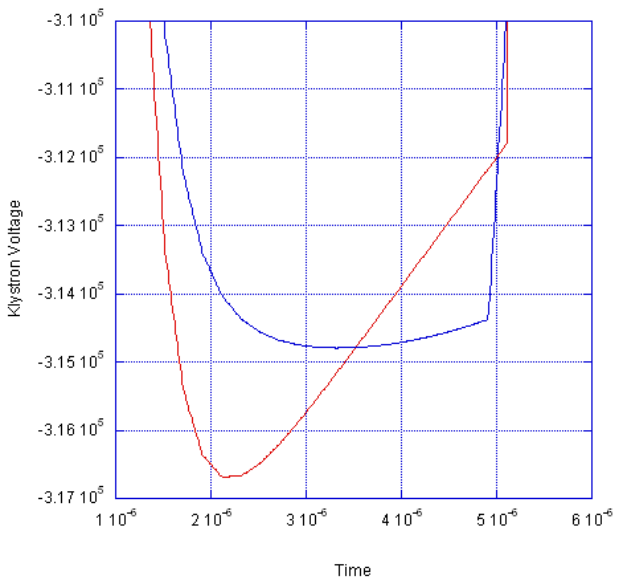

Figure 5. SPICE results of RL compensated (blue), and uncompensated (red) pulses.

STATUS

At this time, the conceptual design of the SSM is complete. All of the major electronics components are either on order or in house. Printed circuit boards for the drive electronics, IGBT boards, diode arrays, trigger electronics and mother board, fault detection board, discriminator are either in design or production.

The mechanical designs of the cell cases and high voltage feeds are complete and the parts are in production. Detailed drawings are in progress for the other mechanical parts for the core stack and solid models for the electronics enclosures and the oil and water systems are in the works. The design of the high voltage tank for the solid state modulator is complete as it will use the same design as the conventional modulator.

The conceptual design of the controls system is complete, and a PLC is in house. The design of the PLC chassis is underway, and some programming has begun.

CONCLUSIONS

Two prototype modulators for FERMI will be built this year. One an upgrade of the conventional modulators used for ELETTRA, the other a solid state inductive adder design. A decision on which modulator technology to use will be made by the end of the year. In 2008, production will begin on five more modulators, and in 2009 the balance will be produced.

REFERENCES

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