CEBAF NEW DIGITAL LLRF SYSTEM EXTENDED FUNCTIONALITY*

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Abstract

The new digital LLRF system for the CEBAF 12GeV accelerator will perform a variety of tasks, beyond field control [1]. In this paper we present the superconducting cavity resonance control system designed to minimize RF power during gradient ramp and to minimize RF power during steady state operation. Based on the calculated detuning angle, which represents the difference between reference and cavity resonance frequency, the cavity length will be adjusted with a mechanical tuner. The tuner has two mechanical driving devices, a stepper motor and a piezo-tuner, to yield a combination of coarse and fine control. Although LLRF piezo processing speed can achieve 10 kHz bandwidth, only 10 Hz speed is needed for 12 GeV upgrade. There will be a number of additional functions within the LLRF system; heater controls to maintain cryomodule's heat load balance, ceramic window temperature monitoring, waveguide vacuum interlocks, ARC detector interlock and quench detection. The additional functions will be divided between the digital board, incorporating an Altera FPGA and an embedded EPICS IOC. This paper will also address hardware evolution and test results performed with different SC cavities.

CEBAF UPGRADE CAVITY PARAMETERS

Frequency	1497 MHz
Loaded Q	3.2*10^7
Lorentz Force Detuning K	2
Cavity Mechanical Sensitivity	300 Hz/um
Cavity Bandwidth	47 Hz
Maximum Gradient	20 MV/m
Microphonics	4 Hz RMS 60 Hz detuning at 8 Hz (stepper induced)
He Pressure Sensitivity	400 Hz/Torr

RESONANCE CONTROL & INTERLOCKS SYSTEM

SC Cavity Resonance Control System

The resonance tuning function is accomplished by mechanical tension of the cavity using two mechanical driving devices, a stepper motor and piezo-tuner a combination of slow and fast control [2]. The stepper-motor driven coarse tuner has a range of +/- 200 kHz and resolution of 10 Hz. The piezoelectric part allows the cavity to be continuously tuned to within 1 Hz of resonance and has a range of approximately 2 kHz. The detuning signal is measured and processed by a digital Low Level RF (LLRF) system and is fed to the resonance control algorithm. The algorithm will drive a high voltage amplifier via a 12 bit DAC. Since the detuning loop bandwidth is limited to f=0.5 Hz, maximum drive signal V_{dr}=150V and the capacity of piezo-element is approximately C=21 μF, the amplifier current should not exceed $i = 2 \times \pi \times C \times f \times V_{dr} = 10$ mA

The CEBAF upgrade cryomodules are designed modulo eight superconducting cavities. Each cavity has an individual tuning system (both mechanical stepper and PZT). The PZT system will be packaged with eight amplifiers in one 19” chassis. Likewise the stepper motor controls will be done in a similar fashion.

ARC Detector Interlock with test source.

A photomultiplier tube (PMT) is used for the waveguide arc detector. The signal from the PMT is sent from the cryomodule, out of the tunnel and conditioned on a custom printed circuit (pc) board. The signal is routed through two paths. The first path is a hardware derived digital I/O signal which is sent to the LLRF chassis to quickly turn off the RF. The second path goes to a fast ADC, where the signal history can be stored. In addition an LED is used to test the PMT periodically.

Waveguide & Beamline Vacuum Interlocks

Vacuum signals from the crymodule are monitored using ion pumps. Ion pump signals are made available to the interlock pc board. Again a digital I/O signal is fed to the LLRF chassis for quick turn off.

Quench Detection System

The quench detector uses a dV/dt (rate of change algorithm) on the cavity gradient. This is processed internally in the LLRF firmware.

Ceramic Window Temperature

A window temperature sensor monitors the IR radiation around the cavity window. The sensor uses a thermopile from where signal is sent to cavity card and LLRF module.

Heater Controls

This system provides the control of the resistive heaters installed in the cryomodules to keep the total heat load and return flow balanced.

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SYSTEM ARCHITECTURE

Fig.1 presents the proposed system architecture for one cryomodule with eight SC cavities. Based on functionality, it was divided into three subsystems, each with their own chassis.

Piezo Drive Chassis consist of eight PZT amplifiers controlled directly by LLRF- Field Control system via 12-bit DAC.

Stepper Control Chassis consists of eight motion controllers and drivers plus one PC104 board computer used for communication and resonance algorithm implementation. All communication with this chassis is performed at the EPICS level.

Interlock/Heater Chassis consists of two FPGA based Cavity Interlock Cards (see Fig.2), each will control signals from four cavities and one PC104 computer board for slow data communication. For fast signals like arc or vacuum are digital lines connected directly to the LLRF module.

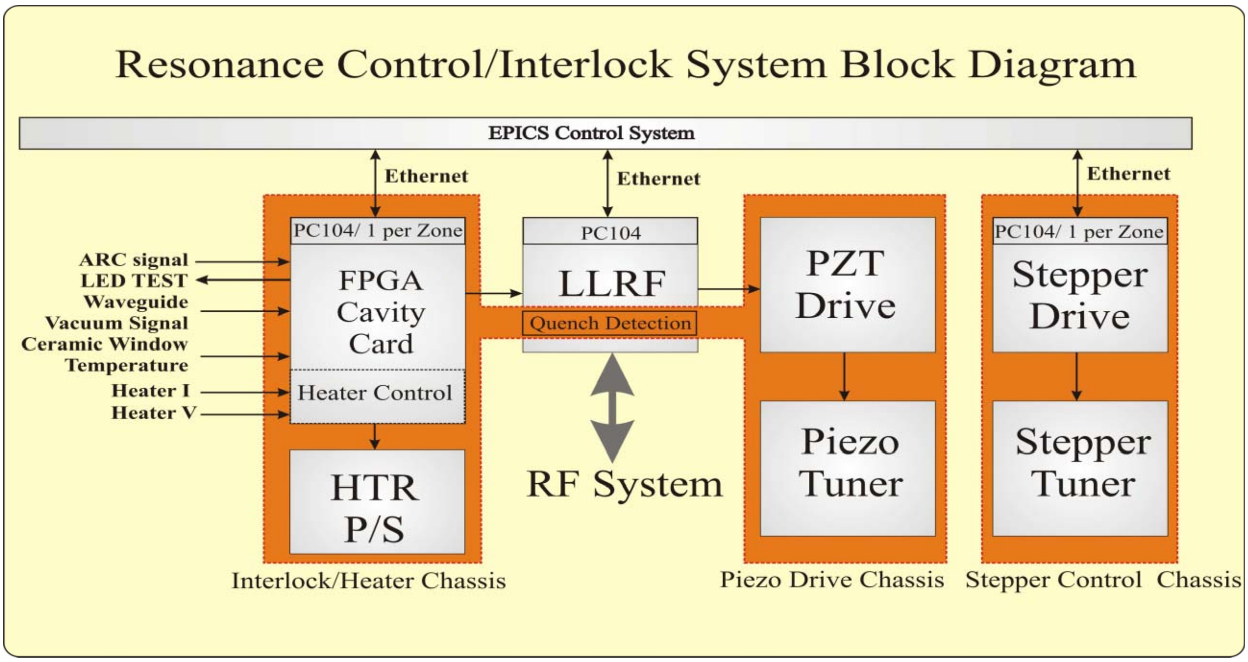

Figure 1: Block Diagram of Resonance Control /Interlock System

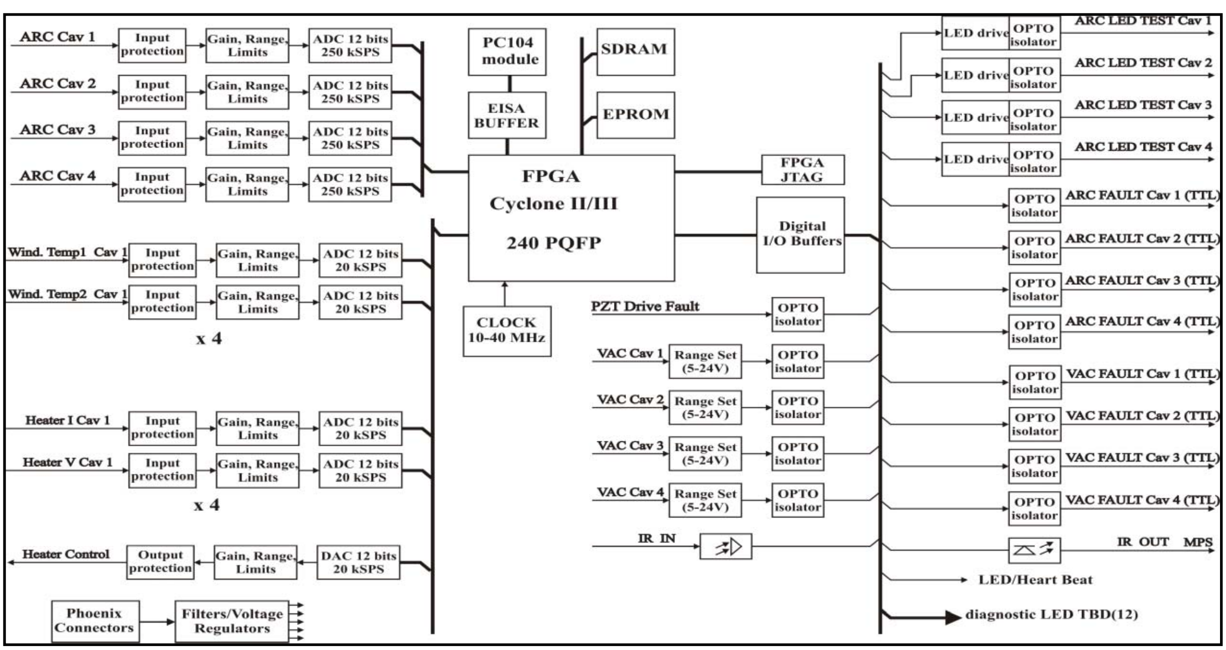

Figure 2: Cavity Interlock Card

SYSTEM FEATURES

Resonance Control Objectives:

- Preliminary cavity resonance tuning to operating frequency of 1497 MHz
- Detune cavity for bypass operation
- Compensate slow drift of frequency due to He pressure fluctuation
- Provides secondary Lorentz Force detuning compensation during cavity turn on where **Self Exciting Loop (SEL)** is a first choice [4].
- Control of stepper motor induced microphonics

Stepper Tuner

Range	+/- 200 kHz
Resolution	4 Hz
Measured tuning per µstep	4 Hz
Phases	A,B
Step/micro-steps	200 full/400 µsteps
Max. speed	60 RPM
Limit switches	yes
Current/voltage	2A per phase/ +24 VDC
Control	TTL, Step&Direction

Piezo Tuner

Tuning Range	2000 Hz
Resolution	1 Hz
Max. voltage	150 V
Full motion	60 um
Full step BW	0.5 Hz
Piezo Capacitance	21 µF
Max. current	20 mA
Modes	Unipolar
Max. output noise	70 mVrms
Control	0-10 V analog

Figure 3 shows PZT amplifier current requirements vs. microphonics detuning and frequency. In our case the worse case scenario is 60 Hz detuning at 8 Hz, caused by stepper motor operation. We have checked that a previously calculated drive current of 10 mA will be sufficient to operate piezo actuator and eliminate the stepper induced microphonics.

Cavity Interlock Card/Chassis

The FPGA based card will handle four cavities. It is intended to use an Altera Cyclone II FPGA . The signal and interlock requirements allow for the use of serial ADCs and DAC. There will be a number of digital input and outputs as well as IR ports for the Fast Shut Down (FSD) interlock. The cryomodule is equipped with eight resistive elements (heaters), however only one heater power supply is needed. A heat load diagnostic will be based on the cavity gradients and a heater voltage/current measurement. Communication to EPICS yet again uses a PC104 as an IOC.

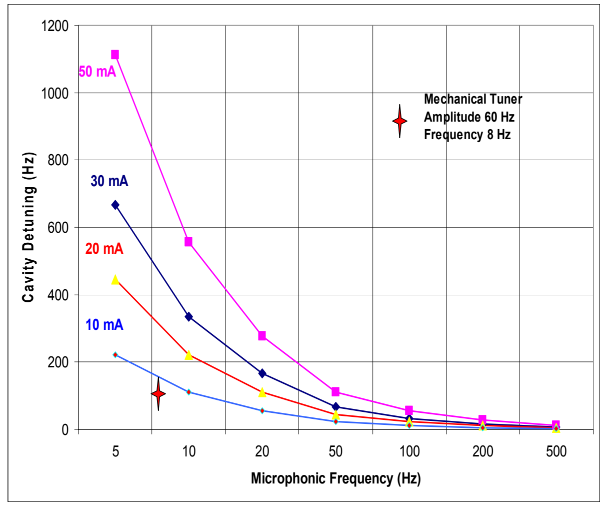

Figure 3: PZT current needed to control detuning

SUMMARY

Resonance Control & Interlocks System consists of variety hardware and software. Presented design was chosen to provide a simple robust and flexible solution. The PC104 standard was selected by the control group as the supported embedded EPICS IOC. Presently we are designing the hardware. Initial tests are planned for 2008.

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