# Design and Measurements of a Damping Ring Kicker for the ILC

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# Summary

- Motivation for the kicker R&D and the most challenging requirements;
- Design of the prototype ILC kicker and discussion of important design parameters;
- Measurement and simulation results for prototype ILC damping ring kicker;
- Conclusions.

# Motivation & Challenges

- The International Linear Collider (ILC) requires ultra fast kickers for the damping ring;
- Deflection angle: 0.6 mrad deflection of 5 GeV electron beam;
- 2005 ILC baseline: considered a damping ring with bunch spacing in the range 3.08ns to 13.85ns, depending on the final configuration.

# Kicker’s Principle Specifications

- The modulators must produce pulses of ±5 kV magnitude, with a width of **≤14 ns** and rise and fall times of **6 ns** or less (2005 specification);
- However a recent baseline suggests a pulse width **≤4.16 ns**, with a burst mode of 3.25 MHz;
- In order not to perturb neighbouring bunches in the bunch train, pre & post pulse kicker field must be close to zero;
- Burst mode of 3.25 MHz, for ≤1 ms, gives an average repetition rate of up to 16.3 kHz.

# Stripline Deflector Plates

- Stripline deflector plates chosen as default technology;
- The permissible rise-time ($t_p$) of the electrical pulse is given approximately by:

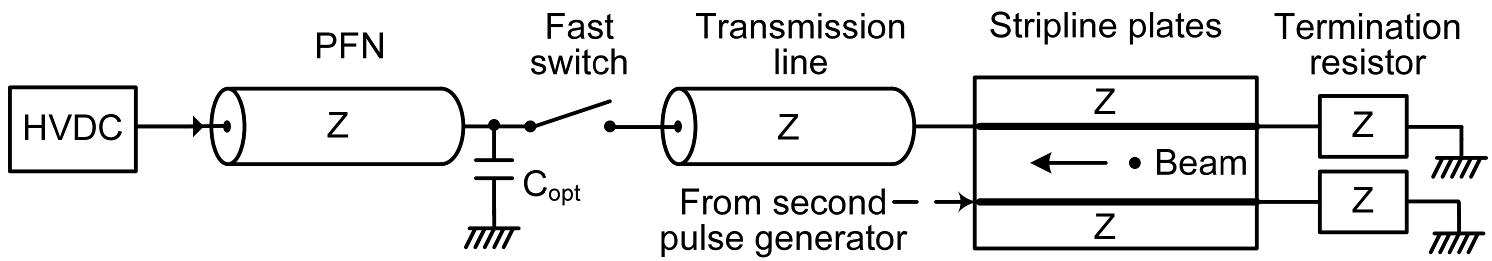
$$t_p = t_b - 2 \cdot l_s / (N \cdot c)$$

where, ($t_b$) is the beam gap and $N$ is the number of sections into which the total stripline length ($l_s$) is sub-divided;

- If $t_b$=6 ns and each set of striplines is 30 cm long ($l_s/N$), i.e. 1 ns fill time, **$t_p$ =4 ns**.

# Pulse Generator

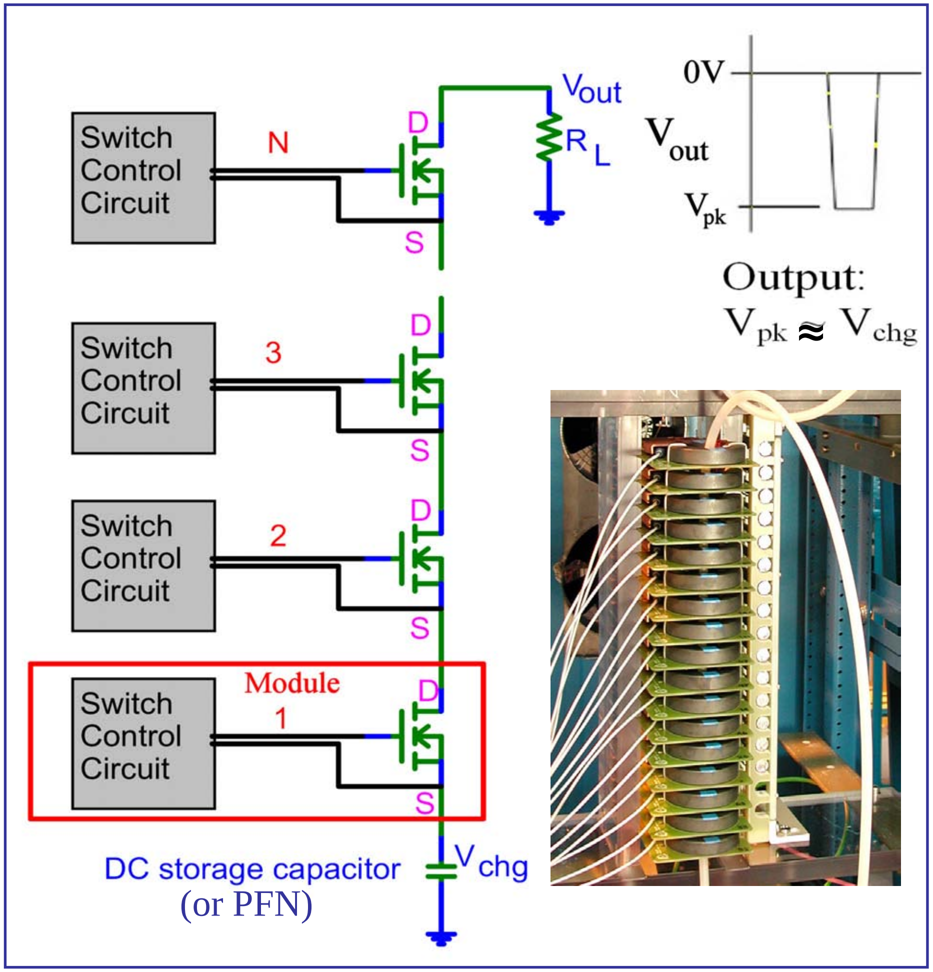
Simplified Schematic of a Possible Kicker System:




Examples of possible technologies for fast switch:

- Stacked MOSFET Switches (SMS);
- Inductive Adder (developed at SLAC/LLNL);
- Fast Ionization Dynistor (FID);
- Behlke MOSFET based switch.

# Stacked MOSFET Switches (SMS)

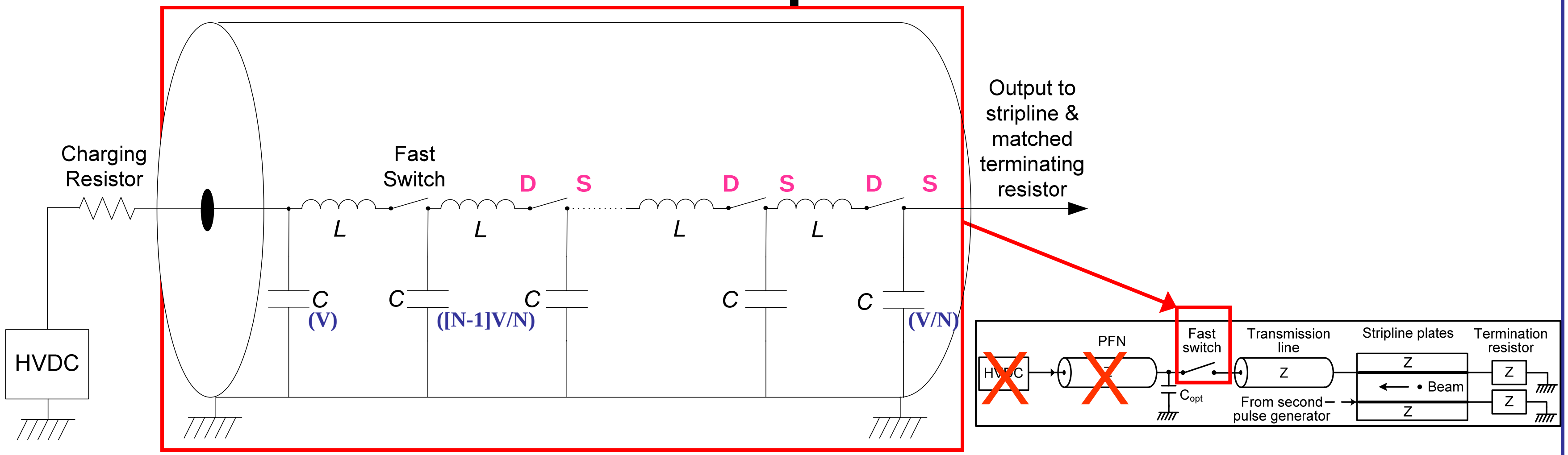



- The DC storage capacitor is charged up to the required high voltage.
- The number of series modules, including redundancy, is chosen based on the switch voltage rating and required high voltage.
- In this example, with a storage capacitor, the MOSFET is gated on to initiate the pulse and gated off to terminate the pulse.
- The switch control unit is at switch source potential, i.e. floating with respect to ground.
- Examples of previous systems:

*500V, 3MHz (cont.), 120ns rise/fall;*

*±12.5kV, 75kHz (cont.), 40ns rise/fall.*

# New Concept for SMS

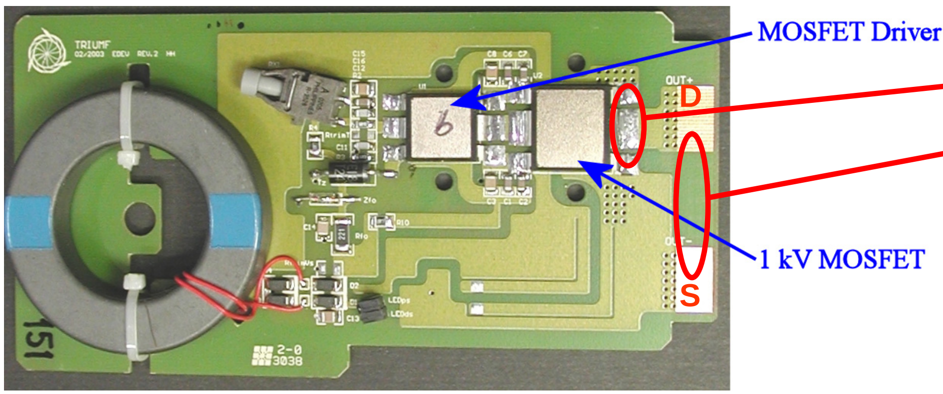



Stacked MOSFET switch is a delay line.

$$Z = \sqrt{L/C}; \quad \tau = \sqrt{L \cdot C}; \quad \text{hence:} \quad \tau = \left( L/Z \right) \;\&\; N \cdot \tau = N \cdot \left( L/Z \right)$$

- Therefore, for a given minimum inductance, the delay of a 100 Ω line is less than that of a 50 Ω line;
- A “delay-line” switch has been configured as ~100 Ω;
- Two parallel delay-lines would give 50 Ω.

# “Old” 1 kV Modules



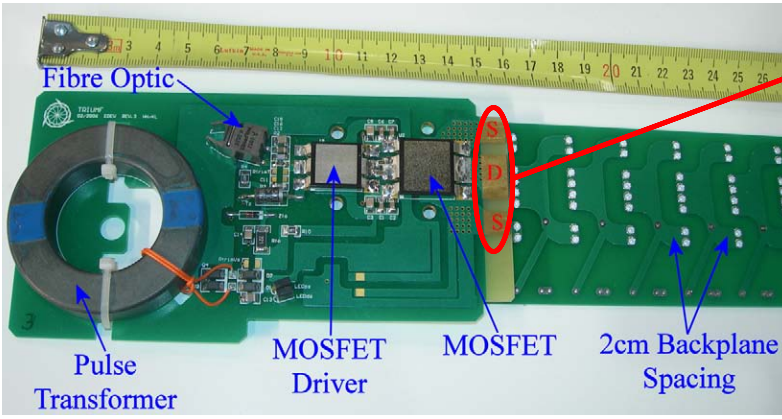

“Old” (MuLan) module design:

- Low inductance output of FET;
- “High” inductance output from module.
- Measured pulses of 4.6kV, with 6ns rise and fall times (10% to 90%) and 21ns width (at the 5% level).

The rise and fall time of the pulse generated are related to:

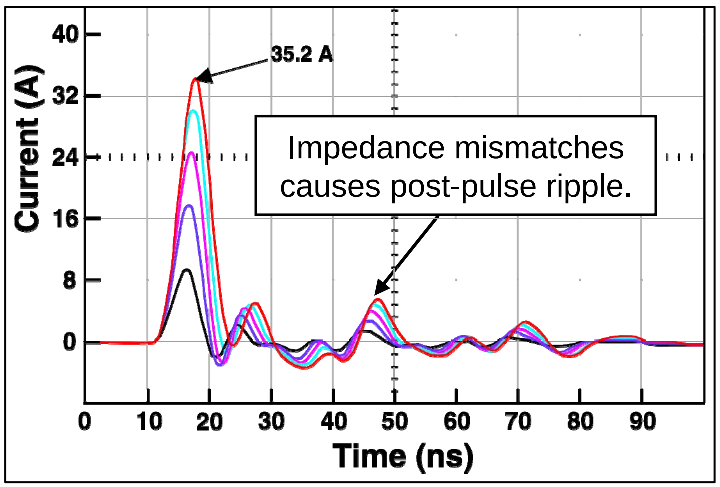
- the intrinsic switching time of each FET (<3ns measured);
- the number of series FETs (15 * 1kV);
- the pulse propagation time through each level of the delay line. $\left[\tau = \left(L/Z\right)\right]$

# "New" 1 kV Modules




"New" (MuLan) card design has:

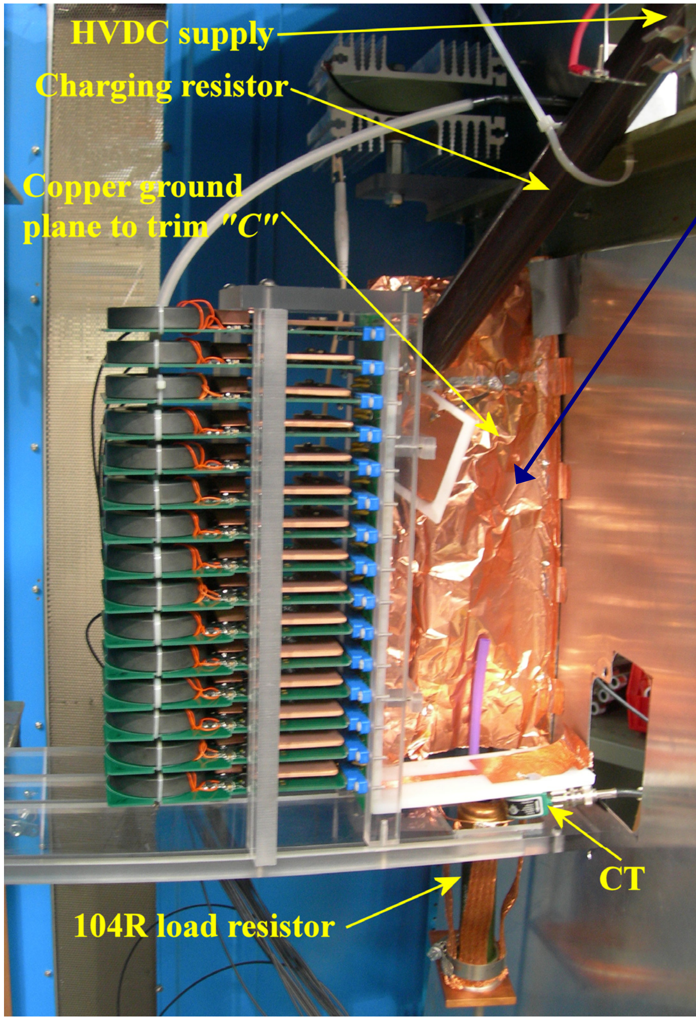
- Low inductance output from module;
- Plugs into low inductance backplane;
- Measurements on stack gave:
  - $\tau$ = 0.21ns/level (direct measurement);
  - L = 30nH±1.7nH/level;
  - C = 1.75pF/level;
  - Hence $\tau$ = 0.23ns/level & Z = 130Ω.



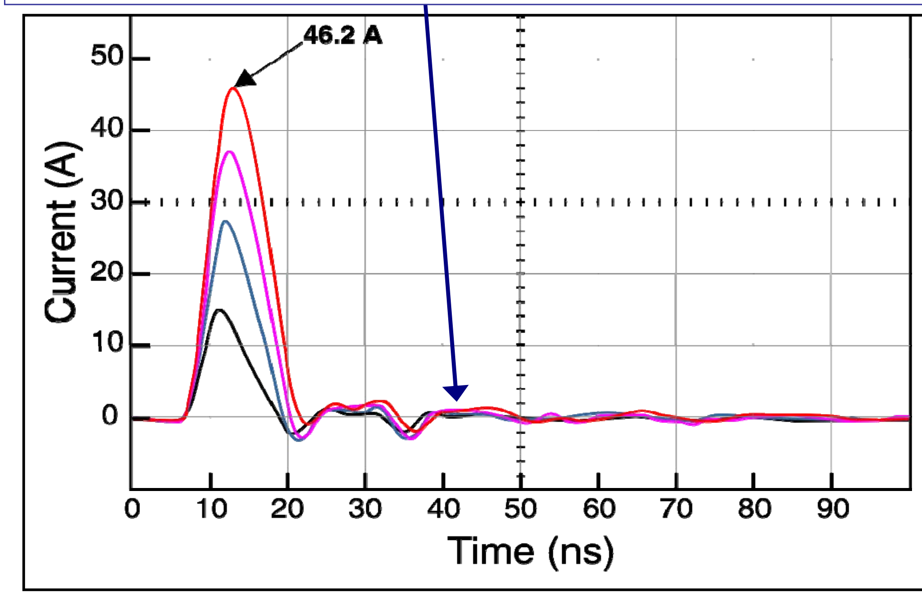

Measured pulses for 2.5kV, 5kV, 7.5kV, 10kV & 12.5kV DC supply; C=1.75pF.

- 35.2A corresponds to **3.66kV** load voltage (104Ω terminator).
- The amplitude is lower than 12.5 kV/2:
  - stack impedance is high (130Ω);
  - ~ 1Ω/FET on-state resistance;
  - *C*, of each level of the delay line, are not all pre-charged to 12.5kV.

# Reduced *Z* of Delay Line



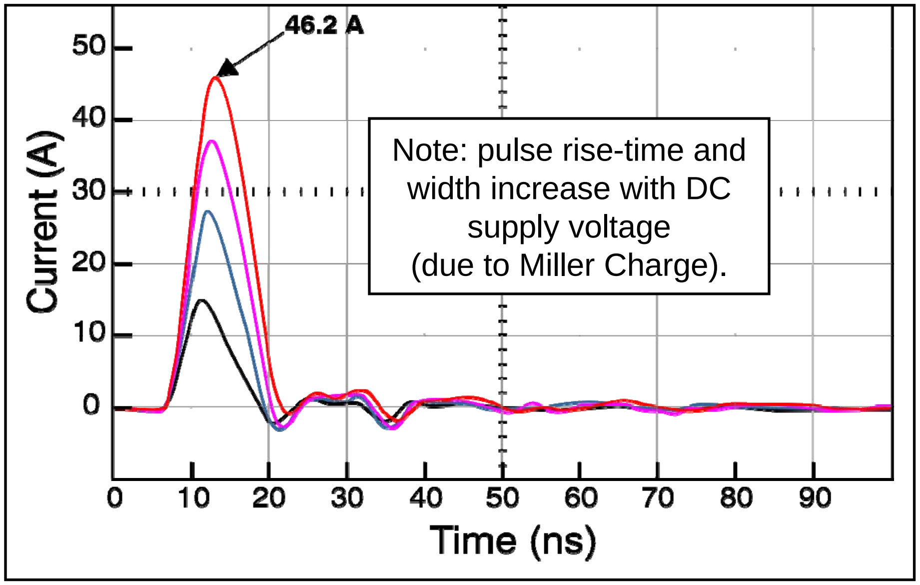

The position of the copper ground plane is changed to minimize post-pulse noise.




Measured pulses for 3kV, 6kV, 9kV & 12.5kV DC supply (C=3.3pF).

46.2A corresponds to 4.8kV load voltage (104Ω load resistor).

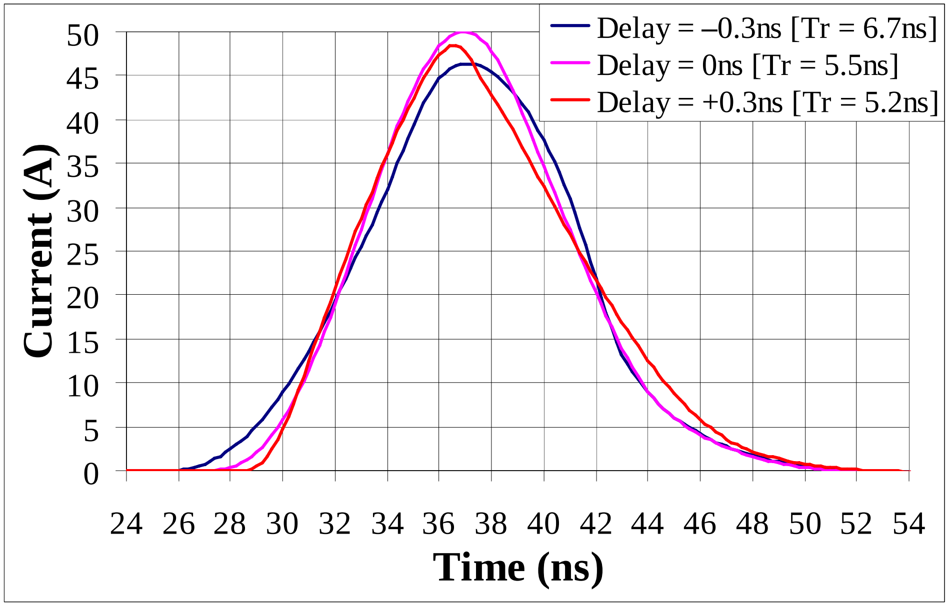
# Parameters of Measured Pulse




Measured pulses for 3kV, 6kV, 9kV & 12.5kV DC supply (C=3.3pF).

- Measured 10% to 90% rise-time is 4.3ns for 12.5kV DC;
- Assuming limited bandwidth (500 MHz) of measurement system does not cause over overshoot, pulse rise-time could be as low as 3.7ns.
- Pulse width at 5% level: 13.7ns for 12.5kV DC.

# Predicted Effect of Relative Timing




Predicted load current with −0.3ns, 0ns & +0.3ns delay between adjacent FETs (12.5kV DC).

Triggering the FETs in sequence, starting at the top of the delay-line, such that:

- there is 0.3ns between FETs turning-on (to compensate for the delay between levels): predicted rise-time = 5.2ns (10% to 90%) [c.f. 5.5ns];
- there is -0.3ns between FETs turning-on: predicted rise-time = 6.7ns (10% to 90%), but faster fall.

# Conclusions

- Pulses of 4.8kV, 4.3ns (10% to 90%) measured rise (~3.7ns actual) and 5.5ns fall and a width of 13.7ns at the 5% level, have been generated at 60kHz continuous;
- This is close to meeting the specifications for the widest (14ns), 2005 baseline, ILC pulses;
- Pulse rise, fall and width can be further reduced by decreasing the stack inductance:
    - by reducing the FET spacing;
    - by increasing the gate drive;
    - using less FETs in series (presently use 1kV FETs !).
- BUT to achieve pulse widths of ≤4.16ns: Behlke switch (see WEPMN068) or FID are more suitable than a delay-line SMS – if they are shown to be capable of the burst-mode operation.